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CAD Tools for Managing Signal Integrity and Congestion Simultaneously

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Abstract

An efficient computer-aided approach is presented that manages delay, signal integrity and routing congestion simultaneously in Printed Circuit Boards and Multichip Modules. The approach is based on use of the Signal Integrity Advisor in conjunction with a global router. These tools have been developed as part of a complete design optimization tool-set spanning partitioning, placement, routing and re-routing. It is also shown how the Signal Integrity Advisor can be used to produce wiring rules for a conventional router.

1 Introduction

In this paper, we describe an improved computer-aided approach to producing a PCB or MCM routing that meets timing and signal integrity constraints across process variations and also in highly congested situations. First, we briefly review existing and proposed approaches. We then present two complementary approaches to producing good routes with examples and conclusions.

Current CAE industry approaches to delay and signal integrity management rely on a mix of simplified linear equations and post-layout simulation. Davidson [1] has developed a human-designer based approach relying on wiring rules and equations that has enjoyed considerable success. Lee et. al. [3] describe an interesting approach for generating routing constraints by solving the Taylor series approximation of the simulated response around a feasible design. However, the constraints they produce must be checked for routability and are limited to first incidence switching. Our approach incorporates routability and can deal also with settling delay.

Previously, [4] [5] we described an approach for generating routing constraints that produces a very flexible rule. However, one step in this approach has exponential computational complexity and is unsuitable for high fanout nets. In this paper, we describe an improved set of approaches that do not use this exponential complexity step.

2 Signal Integrity Advisor

In the ideal world, signal integrity decisions would be made by automatically conducting a fast accurate simulation and using the results to automatically drive the design tools. However, a simulation that includes process variations, lossy lines, or ground inductance models performs too slowly for use while conducting placement or routing.

Instead our approach is based on a detailed pre-characterization [4] [5] of each net class found in a design. For example, consider the 2-receiver net class shown in Figure 1. For such a net class, the signal integrity

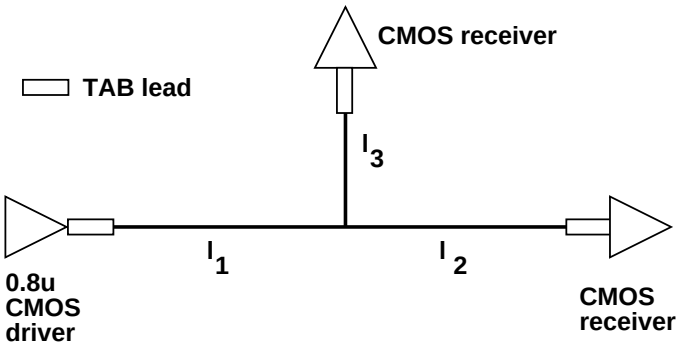

Figure 1: Example of a net class.

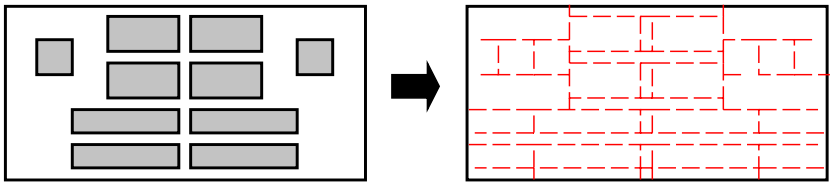

Figure 2: Example of channels identified in a placement.

advisor automatically designs a computer experiment that characterizes circuit responses (the 50% delay, settling delay, undershoot, etc.) across a suitable range of l_1, l_2 and l_3. This characterization only takes on the order of a hundred simulations and is conducted before any design takes place.

Results are stored in tabulated form and are then interpolated to provide a very fast prediction of delay and noise for any particular candidate net design.

3 Global Router

Delay, signal integrity and routing congestion are managed simultaneously through the use of a global router. The steps used in the global router are as follows:

1. A set of channels and edges are identified in the placement, as illustrated in Figure 2. The layout is modeled as a graph where each arc corresponds to a routing channel. (A global route is complete when we know which arcs each net must traverse.)

2. A routing tree is defined as a unique set of arcs through which the routed net must pass. In the second step, the tool identifies which set of routing trees meet signal integrity and delay constraints and have potential to be routable. The tree generator employs the signal integrity advisor's characterizations in order to do this. An example of a set of feasible trees is given in Figure 3.

3. The global routing step is then formulated as a Integer Program as per [2]. The objective of the Integer Program is to determine which feasible trees are to be used for each net so that channel (arc) capacity constraints are met.

4 Producing Constraints for Conventional Routers

The output of the second step could also be used to produce constraints for a single-line detailed router capable of accepting net constraints. In order to do this, the length constraints corresponding to the feasible tree with the longest total wire length are used to generate routing constraints (when a maximum timing constraint had to be satisfied).

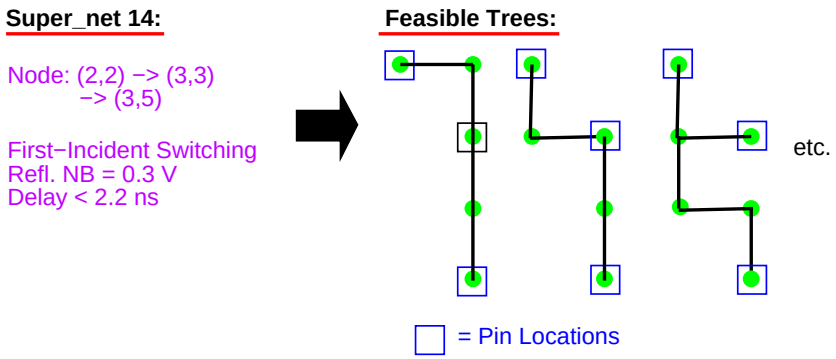

Figure 3: Example of a set of feasible trees for one net to be routed.

5 Example

The routing example models a next generation supercomputer on a 6 × 6 inch substrate with 37 gate arrays chips and 18 high density connectors. The chips are 1.5 × 1.5 cm. with 35 mil TAB leads on a 4 mil pitch. The connectors are placed around the perimeter of the substrate. The net list contains 7,118 signal nets and 14,659 pins.

Two graph models were generated for this design. The first (coarse graph) mapped each chip and edge connector to one vertex in the channel graph. This graph had a total of 64 vertices, 128 edges and 307 supernets. The second (refined graph) model mapped each chip edge to a separate vertex, and each edge connector to one vertex in the channel graph. The resulting graph had 332 vertices, 378 edges and 1200 super nets. The characterizations used 75 and 150 samples respectively for 2 and 3 pin nets. Settling delay to 6% of the supply voltage was used as the delay measure. Several different routing experiments were run by varying the choice of routing trees, channel capacities and timing constraints. The routing trees were screened using the characterizations. The resulting global routes (which all met the channel capacity constraints) were verified by simulating the routing trees for each net. In the worst case 98.05% of trees satisfied the timing constraints, and in the best 99.85% of trees satisfied the timing constraints.

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