Tools to Aid in Wiring Rule Generation for High Speed Interconnects
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Abstract

This paper discusses the construction and application of two tools. The first tool, MetaSim, allows multiple simulation studies to be automatically specified, conducted, and analyzed in such a fashion as to produce wiring rules for layout tools. One of MetaSim's current engines, Transim is a convolution simulator that incorporates a robust, rapid, and accurate method for the simulation of coupled, lossy interconnect structures specified with frequency-dependent parameters.

1 Introduction

The high speed performance of most digital systems is now limited by distributed discontinuities and transmission line effects of packaging and interconnects, and not by the switching speed of semiconductor devices. Among the effects of these distributed circuit elements are: Delay and rise time degradation, ringing, crosstalk noise, metastates, and simultaneous switching noise[1].

In many cases, the quest for higher performance is centering on choosing the most appropriate packaging technology, as well as layout considerations, not just increasing device clocking rates.

However, a number of difficulties are encountered as the circuit designer, layout engineer, and signal integrity engineer seek to design high speed systems.

One primary difficulty is the need for the signal integrity engineer to develop wiring rules to be used in the router [2]. These wiring rules constrain the lengths and spacings (and sometimes widths) on the board or multichip module so that delay and noise requirements are met. Care has to be taken in doing this. If the wiring rules are too lenient, many signal integrity problems will be detected during verification and the board will need extensive redesign. If the rules are too conservative, the router will be overconstrained and available routing area will be used inefficiently. Until recently rules of thumb often sufficed. However, as the rise times in complex CMOS boards and MCMs approach sub-1 ns ranges, the need for more precise wiring rules will dramatically increase.

Precise wiring rules can not be generated from simple analytic expressions for propagation delay as no expression available today can accurately predict the effects of reflection and simultaneous switching noise on delay. Instead, the generation of wiring rules requires multiple simulation studies to be performed across an appropriate range of design and parametric variations. The simulation studies are analyzed in order to characterize the transformation between the physical space (P – lengths, spacings, etc.) and the electrical design space (E – delay, noise). This transformation is then inverted and applied to the placement in order to check it and to formulate wiring rules for the router. We will refer to this set of transformations as the "P↔E transformation".

Carrying out such studies traditionally requires a large amount of engineer time and can be error prone.

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Figure 1: Organization of MetaSim

MetaSim (Meta Simulator) automates the generation, conduct, and analysis of such simulation studies. In this paper, we describe the operation of MetaSim and give an example of its use.

MetaSim interfaces with three simulators, Spice, Cazm and Transim. Transim solves the problem of incorporating transient circuit simulation with nonlinear devices, with transmission line simulation in the frequency domain. For example, this capability is a requirement for thin film MCM interconnect once the skin effect starts becoming important (i.e. when rise times start approaching around 200 ps [?].)

2 MetaSim: A Simulation Generator and Analyzer

MetaSim (figure 1) automates the <simulation set up → simulation execution → simulation results analysis> loop. It thus allows complex relationships between delay and noise requirements on one hand, and technology selection and physical design issues, on the other hand, to be explored with a minimum of human time. MetaSim consists of the following elements (Figure 1):

- A study organizer, which allows variational studies requiring multiple simulation runs to be concisely specified and generated. It also includes specialized simulation file generators for Cazm, SPICE and Transim.
- A waveform analyzer that carries out signal integrity analysis on each set of simulation results and extracts delay and noise data as required.
- Post-processing software that enables relationships to be readily extracted from the analyzed results, and selected waveforms to be retained and viewed.

The nature of these tools will be described further, in section 3, primarily by the way of an example.

In the following sections, we will first describe related work conducted elsewhere, and present an example of MetaSim's use.

2.1 Related Work

The existing approach to wiring rule generation is to make initial estimates and refine on them through multiple iterations of the <specify rules → carry out route → verify → analyze simulations> loop. Although some commercial tools automate part of the analysis they are not able to suggest how to improve the rules. Attempts at this, such as TLTS [7] make very simple suggestions such as 'shorten net' and 'remove receivers'. As better suggestions require that a characterization of the P↔E transformation exist anyway, it makes sense to use this transformation to form good rules initially for as many nets as is reasonable. This will greatly reduce the number of design iterations required, hopefully to one.

The closest existing tool to MetaSim is Adline, which was developed at NTT [5]. It is only available in Japan. Adline includes in its simulator, the ability to specify multiple simulations for some structures. With Adline, as with MetaSim, it is also possible to study the effect of process variations by automatically carrying out multiple simulations. The main distinction between Adline and MetaSim is that MetaSim offers far greater flexibility in the range of studies that can be undertaken. MetaSim can also be easily integrated with any simulator while Adline is integral with one simulator.

3 Example of the Application of MetaSim

MetaSim is applied before layout by taking a net, or set of nets, that are likely to require layout constraints and conducting studies on them. For example, here, we will consider the set of nets that have one output and four inputs, and the output may, or may not be, part of four simultaneous switching outputs. The interconnection network topology is described as a set of branches and stubs, in a daisy chain configuration, as shown in figure 2. The circuit technology is 0.8μm CMOS, and the packaging technology, a polyimide-dielectric thin film MCM, with copper interconnect, and non-fan-out-TAB chip attach.

For the purposes of this paper all of the branches shown in figure 2 will be set at the same length as will the stubs. This is only done to make the results presentable. Part of the study command file that specified the studies that produced the results presented here is shown in figure 3. Part of the 'data file' is also presented. In this study, three network related components are varied independently, the driver circuit model, the branch length and stub length, in order to specify a total of 32 simulation runs. The command language is actually a formally defined programming language with many constructs other than the ones

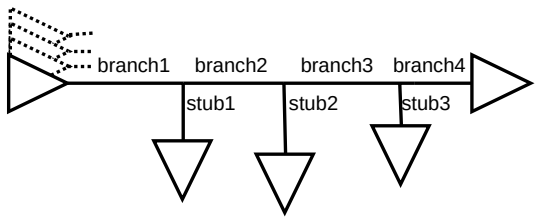

Figure 2: Network topology to be analyzed. The output driving the net might have up to three other outputs switching with it. The user can specify any circuit model for the ground and power connections and can specify driver skew.

Extract from command file:

```
contr
  for ($branch = 1e-2 4e-2 1e-2 incr)
  for ($stub= 1e-3 2.9e-2 4e-3 incr)
  do{
    undsht = "5"
    delay  = "1" "5" 0.23
    delay  = "1" "5" 0.734
    }
```

Extract from 'data' (generic simulation specification) file:

```
Branch 1:

Brch_type_1 bstrip Brch_length_1 $branch
Height1A_1 10e-6 Height1B_1 20e-6 Thick1_1 5e-6
Width1_1 17e-6 Er1_1 3.5 Er2_1 3.5
Brch_load_1 non-loaded
```

Figure 3: Part of the command and data files used to specify the study described here.

shown including random generation constructs.

The 'data file' shown in figure 1 is a generic simulation specification file that lists all of the elements to be simulated as a network of objects (eg. a branch in a transmission line is an object) with certain properties associated with them. The "$" variables that appear in the command file also appear in the data file. The study organizer then produces appropriate substitutions for each simulation run and passes the modified data file to the program that generates the actual simulation file (or directly to Transim, as a Transim file is already described in object-orientated terms). Discontinuities, such as vias, bends, and crossovers can also be specified in the data file, as can coupled lines and connectors.

The 'do' statement specifies what analysis needs to be carried out on the simulation results. In this case we wish to know the peak undershoot at node "5" (the last receiver in the chain) and the delay from the driver output, node "1" to this receiver. We are not interested in the 50% delay, however. As this is a data line, we wish to know when it is safe to latch the data, that is when the noise on the signal line has settled to the point that the combined reflection and transmitted simultaneous switching noise has settled to less than that fraction of the noise margin that the noise budget allows for it, as shown in figure 4. In the command file shown in figure 3, the maximum allowed combined reflection and transmitted simultaneous switching noise for a high-to-low transition is 23% of the voltage swing. Many other analyses can be done, including overshoot and metastate analysis. It is also possible to specify other noise budget and delay specifications.

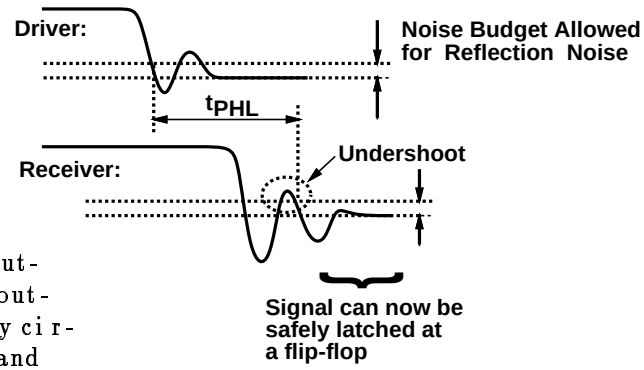

Figure 4: Definition of delay to include settling time for noise.

Figure 5 shows some of the results obtained from running MetaSim with Cazmas the simulation engine. An important result demonstrated through these examples is that despite the non-regular shapes generally found in simulation waveforms, the trends in the settling time plots are generally regular. The steps in the plots are the only irregularities. The steps arise when a change in length suddenly makes the peak undershoot voltage edge past the noise threshold. This result is important because it means that, as long as these steps are located, it is not necessary to carry out a large number of simulations in order to characterize the physical design space being considered. It also means that piecewise linear equations could be fitted. All of the studies we have carried out so far verify this result (sometimes piecewise polynomial equations would be required, however) though we cannot claim to have analyzed every possible situation. Sensitivities would be expected to increase with pulse edge rate, for example.

The physical design tools would then use these re-

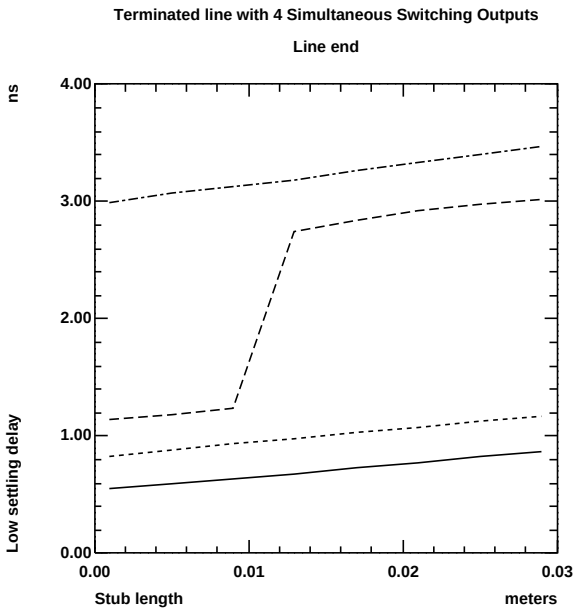

Figure 5: Total high-to-low delay between the ends of the line for different branch and stub lengths, for series terminated lines. (Solid line = 1cm branch lengths, short dashes = 2cm, long dashes = 3 cm, dash-dot = 4 cm.)

sults to adjust the placement and specify wiring rules. For example, if the total high-to-low delay between two chips at opposite ends of a net had to be less than 1.0 ns, then these results can be used by the placement tool to indicate a requirement for a parallel termination in order to control the excessive noise. If the two pins in question were just under 8 cm apart then a maximum stub length of 1 cm is permitted as long as the first to last pin length is 10 cm. The placement tool can then determine if it is likely that the router can meet these constraints. If there is a high likelihood that it can, then these constraints are passed to the router as a wiring rule. If it is likely that it cannot, then the placement tool suggests an improved placement. Automating this procedure should be straightforward.

4 Transim

Transim uses a convolution technique to allow mixed simulation of linear elements specified in the frequency domain and non-linear elements that need to be simulated in the time domain. In this section of the paper, we will first briefly discuss the operation of the convolution simulation core before presenting its operation as a complete simulator.

4.1 Related Work

Several approaches to this problem have been tri with varying degrees of success. The Laplace Tra formtechnique is good at handling multiconduct transmission line systems and while it is more cient than the convolution technique, its limite ity to handle frequency dependent effects and pro lems dealing with nonlinear terminations restric usefulness. The Method of Characteristics [1] is tively easy to use with conventional circuit simul but it is restricted to lines described by RLGC pa eters. Other techniques for simulating distribut ement systems have recently been reviewed by Djor jevic et al [3] and Schutt-Aine and Mittra [6].

In one of the convolution techniques the freque domain network description is converted to a tir domain description using a Fourier transform. Wh this technique can handle arbitrary lossy coup networks, aliasing in the frequency-domain to ti domain transformation can cause appreciable err in the simulated transient response.

4.2 Convolution Simulation Core

Our approach is similar in some respects to th of Djordjevic et al, expect that where Djordjevi use admittance (Y) parameters to characterize frequency dependent network, we use the scatteri (S) parameters. As the S parameters vary only be tween -1 and +1, we overcome the dynamic range problems with the other convolution method's a proach. S parameters describe the relative amplitude and phase of the forward and backward traveling waves at each port an at each frequency on a transmission line of charac istic impedance Z_{ref}.

Integration into a transient circuit simulato requires that the description of the transmission system be in terms of total voltages rather than traveling wave components implied by use of S para eters. This can be achieved by terminating each p in its reference impedance so ensuring that ther no reflections at the ports of the distributed net

Now the total transient response of any linear net fed with voltage sources at the ports of the network can be determined by convolving in time these voltages w the Dirac impulse voltage responses at each exte port of the network. More explicitly, the total transient response at port i of a transmission line sy

Figure 6: Complete Structure of Transim Simulator.

to a total voltage $V_i(t)$. With output impedance Z_m at each port is [8]

$$V_i(t) = \sum_{j=1}^{N} \int_{-\infty}^{t} g_{ij}(t-\tau)\, E_j(\tau)\, d\tau = \sum_{j=1}^{N} g_{ij}(t) \star E_j \qquad (1)$$

Here the symbol $\star$ denotes convolution, N is the number of external ports in the transmission line system and

$$g_{ij}(t) = \frac{1}{\Delta t}\mathcal{F}^{-1}[G_{ij}(\omega)] = V_i(t)/E_j(0) \qquad (2)$$

is the impulse response at port i and at time t to a Dirac delta source at port j and time zero, In (2)

$$G_{ij}(\omega) = \begin{cases} (1+S_{ij}(\omega))/2 & i=j \\ S_{ij}(\omega)/2 & i \neq j \end{cases} \qquad (3)$$

is the frequency-domain Green's function from port j to port i at radian frequency ω and $\mathcal{F}^{-1}$ the inverse Fourier transform. Finally, $\Delta t = 0.5/f_{max}$ the time increment, f_{max} is the highest frequency component of $G_{ij}(\omega)$.

Based on these techniques, Transim has been implemented [8]. Essentially, the interconnect structures to be simulated, are partitioned into a collection of linear, frequency dependent parameter structures, and non-linear circuit structures (including time dependent voltage and driver sources). Simulation proceeds by minimizing the difference between the estimated voltages at the terminals of the non-linear elements and the voltages at the terminals of the linear elements, as determined via convolution.

4.3 Operation as a Packaging Simulator

The complete structure of Transim is shown in Figure 6. Transim is a model-independent simulator. Instead modeled elements are represented in terms of admittance matrices. Thus new models for both interconnect structures and drivers and receivers can be added quickly. From the Y-matrices corresponding to all of the modeled elements a complete Y-parameter matrix is constructed. An important step is the reduction of this matrix to a $M \times M$ admittance matrix, where M is the number of nonlinear nodes. After reduction, the Y-matrices are converted to SPICE drivers and then an FFT is carried out in order to obtain the Green's functions. These are then used in the convolution.

5 Conclusions

MetaSim can be used to characterize the transformation between the physical design space (line spacing, etc.) and electrical design space (delay) before any layout is done. The layout tools can then apply this transformation to the placement in order to suggest placement improvements and also to formulate wiring rules (routing constraints) for use in a router. MetaSim could also be used for other physical design scenarios where analytic delay and noise models are inadequate, such as high speed DRAM design and packaging technology selection. It is very flexible and could be integrated with any simulator.

As it is used for a-priori analysis, MetaSim would conduct more simulations than a post-layout simulator would be required to. This suggests that increased run time might be an issue of concern. There are three counterpoints, however. First, in high speed design avoiding the need for multiple iterations of the design will save more user time and computer time than would be spent in using MetaSim up front, and will also lead to more efficient use of board space. Second, MetaSim is very efficient with the human designer's time. Third, initial results indicate that the transformation is generally regular and thus a good characterization can be obtained with a small number of randomly generated results, as long as the irregular points are found.

Transim is one of the three simulation engines currently in MetaSim. It is a convolution-based simulation that has solved a number of the problems usually found in such simulators. It has been developed as a complete packaging simulator.

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