MODELLING INTERCONNECT YIELD IN RECONFIGURABLE CIRCUITS

Indexing terms: Integrated circuits, LSI, Modelling

Reconfigurable interconnect is required to implement defect-tolerant circuits. The impact of this wiring on yield is usually either ignored or overstated. A method is presented here that allows the determination of the yield impact of the interconnect in reconfigurable circuits through the expanded use of critical area parameters.

Introduction: Ultra-large-scale or wafer-scale arrays require defect tolerance for an improved manufacturing yield. This is achieved by providing spare processing elements (PEs) that are configured into the array, as required, using a flexible interconnection scheme. Additional wiring and switches are required to do this. Faults in this interconnect are likely, and thus their impact on array yield should be determined.

Some previous studies have assumed that any wiring fault will lead to complete array failure.[4] Many other studies have assumed that interconnect faults are extremely unlikely and thus can be ignored. In many arrays the wiring area can easily consume over 10% of the total area, and thus its yield contribution should be properly accounted for. In this letter a method of accounting for these faults in the yield model will be presented.

Yield model for defect-tolerant arrays: The yield of a defect-tolerant array can be expressed as[4]

$$Y = \sum_{k=0}^{\infty} \frac{\Gamma(k+\alpha)}{\Gamma(\alpha)} \frac{(1/\alpha)^k}{(1 + D_0 A/\alpha)^{k+\alpha}} \frac{(D_0 A_{mod})^k}{k!} P_{kNR} \qquad (1)$$

where k is the number of faults in the area that can be repaired A_{mod}, A is the total critical area subject to defects, D_0 is the average defect density, α is the clustering parameter, and P_{kNR} is the probability of repairing the array with N PEs, R of which are spare. (Note that a fault in the area $A - A_{mod}$ will lead to a complete array failure as it cannot be repaired.)

Other area parameters can be included depending on the fault modes possible. For example, if there was a fault mode that could affect a whole row, and spare rows were provided, then another reconfigurable area, A_{row}, should be included. A_{row} is the critical area that can be affected for whole row faults.[6]

P_{kNR} is, in part, a function of the reconfiguration scheme. No reconfiguration scheme can make perfect use of all its spares, and this is reflected in P_{kNR}. We can determine P_{kNR} through simulation of the reconfiguration schemes under different fault patterns.

Accounting for interconnect faults: A fault in the inter-PE wiring or in the control circuits that govern reconfiguration can have an effect ranging from none at all to complete array failure, depending on its location. One way to account for this is to simulate the array in the presence of both interconnect and PE faults, and adjust P_{kNR} accordingly. A slightly less accurate, but much easier to use, method will be presented here.

The effect of wiring faults can be introduced into the yield model by assuming that wiring faults fall only into one of the following categories:

(1) A wiring fault that can be treated as a fault in one associated PE.

(2) A wiring fault that leads to complete array failure ('array kill').

(3) A wiring fault that produces no effect at all.

(4) A wiring fault that can be treated as a fault affecting a predetermined number, or patterned grouping, of PEs.

The first effect can be modelled by adding the appropriate wiring area to the PE area; the second by adding area to the array area; and the third by adding no area to any yield model parameter. The fourth is a more complex situation that will be described in detail. The justifications for choosing these categories are as follows:

(*a*) Many faults, particularly for near-neighbour-only connections, result in limiting access to one PE only. If the fault is in the connecting wire then access is limited from one direction only. If the fault is in the reconfiguration controller then all access to the PE is most likely denied. Some such controller and interconnect faults may limit access to several PEs. These multi-effect faults can only be approximately handled in the model by exaggerating their area, or by grouping them in the fourth category. On the other hand, a fault resulting in the removal of one PE may result in the removal of several PEs from the array. This could happen, for example, when no further replacement PEs are available for that row and a whole column has to be removed. This last effect is handled automatically by the simulation results embodied in P_{kNR}.

(*b*) Many wires, such as power and clock lines, are distributed over the whole array and a failure in these will usually result in an array kill. In some reconfiguration schemes a fault in a section of the interconnect may result in an array kill. Generally it is desirable to minimise the array kill area.

(*c*) Owing to their role as redundant PE connectors, most of the inter-PE wires are not used in any one reconfigured array. Thus many wiring faults will occur in inactive wires and have no yield effect.

(*d*) Except for the simplest reconfiguration schemes, most of the inter-PE wires provided are not used because they are included to enable redundancy and thus many wiring faults result in no yield effect.

(*e*) The final case may arise in situations where a row or column is affected by a single failure. For example, in many arrays an interdigitated comb pattern is used for distributing power and clocks. A failure in one of the comb fingers will mean that on average half of the associated row or column is lost. Note that this is not necessarily the case in all arrays. In Reference 3 the power and clock distribution can withstand one failure in each column. Some interconnect failures can also result in the complete loss of a row or column.

Case 4 cannot be adequately handled by adjusting A_{mod}, but is best covered by introducing A_{row} and/or A_{col} as is often done for memories.[6]

For a power failure in an interdigitated, non-fault-tolerant power distribution scheme, if the loss of part of a row can be effectively contained to that row then, on average, half of the PEs in a row will be lost. For the scheme that will be analysed below, power and clocks would not be fed along the rows because loss of power in part of one row meant that approximately the same portion of all the other rows would be unusable. On the other hand, partial loss of a column will have a smaller impact on yield.

As an example of how to determine values for area categories 1–3 above, consider the mesh array reconfiguration scheme[1,5] given in Fig. 1. In this scheme, a mesh is mapped onto a faulty array by bypassing faulty PEs within each row and by steering the columns around these faulty PEs. The contributions of wiring area to the different areas required for the yield calculations are determined as follows.

The array kill area is

$$A_{kill} = A_2 + A_4(1 - UY) \qquad (2)$$

where the wiring areas A_i are determined by reference to Figure 2, Y is the yield of the PEs, and U is the utilisation of the PEs. The contribution of A_4 is determined by consideration of what percentage of these areas is actually required in a reconfigured array. The areas A_i refer to wiring area over the whole array, not just the wiring area around each PE. The PE area is

$$A_{PE} = A_1 + A_5 UY + \tfrac{1}{3} A_3 UY \qquad (3)$$

In this case $\frac{1}{3}UY$ of the wiring area A_3 is used (note: UYN PEs are used, where N is the number of PEs in the array.) A_{PE} and A_{kill} are related to the area parameters used in eqn. 1 by $A_{mod} = NA_{PE}$ and $A = A_{mod} + A_{kill}$.

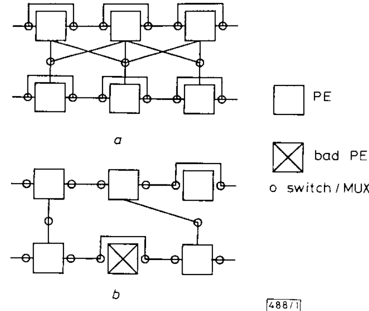

Fig. 1 *Mesh array reconfiguration scheme showing (a) all wiring and (b) example with faults*

a Reconfigurable array *b* Reconfigured array

As can be seen above A_{kill} and A_{PE} are adjusted simply by adding that wiring area actually required.

Using these terms for area in a yield calculation results in a self-referential equation (the individual PE yield Y is required to determine the utilisation U and thus the array yield or $E(P)$). This is not a major problem as the wiring areas involved are relatively small, and Y and U need only be determined approximately. If more accuracy is required then the calculation can be iterated.

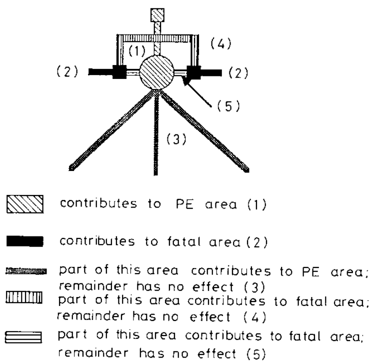

Fig. 2 *Contribution of wiring areas to yield areas*

Conclusions: A significant portion of the area of a defect-tolerant array may be used by the reconfigurable interconnect. Yet its contribution to array yield is often ignored or greatly misrepresented. A simple way to include the yield effect of the interconnect is to adjust the area parameters used in the array yield model. An example of how to do this for an actual array is given. Further examples can be found in Reference 2.

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CRITICAL THICKNESS IN STRAINED-LAYER GaInAs/GaAs QUANTUM WELL LASERS

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The critical thickness in strained-layer GaInAs/GaAs quantum well lasers was studied by measuring the dependence of the threshold current on the number of quantum wells. The critical thickness for 20% In composition was found to be around 30 nm, which is twice as large as predicted by the Matthews–Blakeslee model.

Introduction: Advances in epitaxy technology, such as MBE and MOCVD, make the commensurate growth of strained layers in mismatched material systems possible.[1] This has generated widespread interest in strained layer GaInAs/GaAs quantum well (QW) lasers, which extend the available wavelength range beyond GaAs towards longer wavelengths. Very low threshold current density broad area lasers have been achieved in this material system.[2] The total thickness of the GaInAs active layer in these lasers is below the critical thickness predicted by the Matthews–Blakeslee model.[3] In this letter, we demonstrate that relatively low threshold current density can be achieved in strained layer GaInAs/GaAs multiple quantum well (MQW) lasers with a total GaInAs thickness twice as large as the Matthews–Blakeslee critical thickness. Additionally, results of a study on the stability of these lasers at high temperature are presented and compared with the behaviour of GaAs/AlGaAs QW lasers under similar conditions.

Growth: The GaInAs/GaAs QW material was grown by molecular beam epitaxy (MBE) on a Varian GEN II machine. Typical laser structures with a single quantum well (SQW) and four quantum wells (4-QW) are shown in Fig. 1, exhibiting a separate optical confinement structure. The $Ga_{0.8}In_{0.2}As$ well width is 7·5 nm and the GaAs barrier width (for the MQW structures) is 8 nm. The thickness of both the upper and lower GaAs guiding layers is 125 nm. The QW and the guiding layers are undoped. The thickness of both upper and lower $Al_{0.2}Ga_{0.8}As$ cladding layers (doped with $5 \times 10^{17}\,cm^{-3}$ Be and $1 \times 10^{18}\,cm^{-3}$ Si, respectively) is 1·3 μm. The p^+ GaAs contact layer (doped with $> 1 \times 10^{19}\,cm^{-3}$ Be) of 200 nm thickness is placed on the upper cladding layer. For all the laser structures with different numbers of QW (1, 3, 4, 5 and 6) that were grown in our study, the layer thicknesses of the wells, the barriers, the separate guiding layers, and the cladding layers stay the same. The growth temperature for the GaInAs QWs was 530°C, for the GaAs guiding layers 600°C, and for the AlGaAs cladding layers 680°C. The GaAs barrier layers between the GaInAs wells in the MQW structures were grown at the same temperature as the GaInAs (530°C). The V/III beam equivalent pressure ratio was about 20 for all layers.