# An Arbitrary Waveform Stimulus Circuit for Visual Prostheses Using a Low-Area Multibias DAC

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***Abstract*—Attempts are underway to construct a retinal prosthesis to recover limited vision for blind patients with retinitis pigmentosa using implantable electronic devices. These microchips provide electrical stimulation to damaged retinal tissues using an array of stimulus circuits. This paper describes improvements to conventional circuit designs with significantly decreased implementation area and the ability to support arbitrary stimulus waveforms where an array of such stimulus circuits is required. This yields greater spatial resolution in stimulation owing to more stimulus circuits per chip area. Also introduced are digital-to-analog converter gain prescalar and dc-offset circuits which tune the stimulus circuits to an optimally effective range due to variation in retinal degradation. The prototype chip was fabricated by MOSIS in 1.2-$\mu$m CMOS technology.**

***Index Terms*—Age-related macular degeneration, digital-to-analog converter (DAC), electrical stimulation, retinal prosthesis, retinitis pigmentosa, visual prosthesis.**

## I. Introduction

AGE-RELATED macular degeneration (AMD) and retinitis pigmentosa (RP), which are among the leading causes of blindness [1], affect over 10 million people worldwide through progressive photoreceptor loss (rod/cones) in the retina [2]. Attempts are underway to construct a visual prosthesis to recover a limited sense of vision for these patients using implantable electronic devices to electrically stimulate existing viable retinal tissues using an array of on-chip stimulus circuits. Acute medical experiments have determined that the effective impedance of RP and AMD degenerate retinal tissue at the stimulation frequencies of interests (40–60 Hz) varies around a value of 10 k$\Omega$ [3] and could require stimulus current amplitudes upwards of 600 $\mu$A [4]. The demonstration that direct electrical stimulation of retinal ganglion cells can create visual sensation in patients has been shown clinically [5]. Controlled biphasic charge-balanced current signals in this range delivered to degenerate retina can elicit the perception of phosphenes, or spots of light, in blind patients. By stimulating several adjacent locations simultaneously on the retina patients can experience multiple phosphenes which convey an image when viewed collectively. Patients have been able to recognize alphabetic characters and other simple patterns when stimulated by a small array (e.g., $3 \times 3$ or $5 \times 5$) of retinal electrodes. This opens the possibility of an electronic prosthesis to bypass the defective photoreceptors. Several studies have investigated the effectiveness of low-resolution vision [5], [6]. Results from [7] indicate that larger electrode size/spacing increases the difficulty in detecting facial features. Images of only two gray levels are insufficient for resolving facial detail. A reduction in electrode count from $25 \times 25$ to $16 \times 16$ requires more manual "scanning" across the scene to offset "tunnel vision." This was exacerbated when increasing the pixel dropout percentage. Based on these insights, innovative circuit topologies yielding greater spatial or intensity resolution through reduced circuit area would be valuable to visual prostheses. Furthermore, differing degrees of retinal degeneration among patients requires various forms of stimulation patterns.

Numerous stimulators designed for visual prostheses [8]–[10] use current-mode digital-to-analog converters (DACs) which switch currents weighted in powers of two. Although this does not provide linearity as good as with "thermometer-coded" DACs [11] and requires the same amount of analog circuitry [12], the binary-weighted DAC requires no decoding of the digital input, justifying its popularity in implantable devices where area is a premium. The major disadvantage of both DACs for implantable stimulators is an implementation area which grows exponentially with resolution.

In [13], a DAC implementation is reported with circuit area reduced to 0.01 mm$^2$ in 1.2 $\mu$m for 5-bit resolution in which device widths and lengths are varied together to achieve a power-of-two current weighting. Since tracking performance between transistors in current mirrors can suffer from $V_t$ variation, process variation in device geometry, or from channel length modulation [14], this approach may lead to nonmonotonicity in the DAC transfer function. The *multibias* DAC offers an alternative where devices of fixed width and length are used in a low-area topology while retaining low integral nonlinearity (INL) and differential nonlinearity (DNL). INL is a measure of deviation of the actual transfer function from a straight line whereas DNL is a measure of deviation of the actual least significant bit (LSB) step size from the ideal step size. The circuit area scales linearly versus number of bits instead of exponentially, yielding more stimulus circuits per chip area and thus, greater stimulus resolution.

This paper is organized into six sections. Section II introduces the novel multibias concept and how this leads to a

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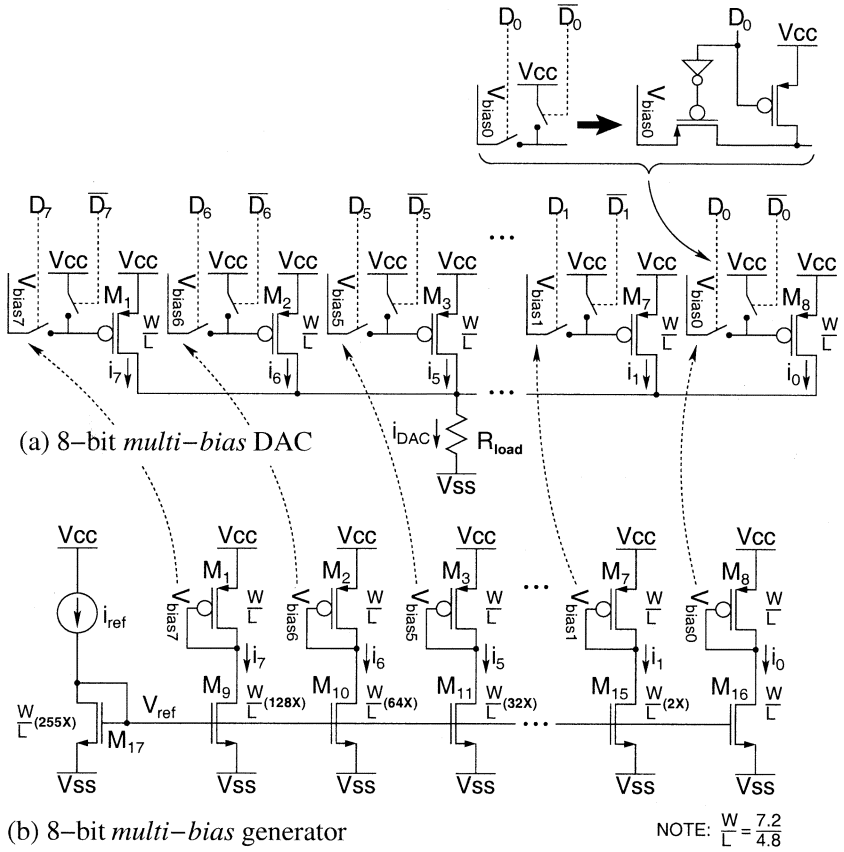


Fig. 1. Multibias DAC concept introduced with simple pMOS current mirrors.

lower implementation area over conventional stimulus circuits. Section III discusses circuit implementation. Section IV provides experimental measurements and additional insights from circuit simulation. Section V covers improvements and design enhancements in future revisions, with concluding remarks in Section VI.

## II. Proposed Improvement: Multibias DAC

Currents in the binary-weighted DAC derive from a shared field effect transistor (FET) gate bias which is produced in a single reference branch. This is distributed across the DAC branches to reproduce the output currents. The power-of-two weighting of the branch currents is controlled using device geometries, defined as $i_n = K(2^n W/L)(V_{\rm ref} - V_t)^2$, for $0 \le n \le N$ (neglecting channel length modulation). For an $N$-bit DAC of simple current mirrors, this requires $2^N - 1$ transistors of size $W/L$. The modification developed for the multibias DAC is to replace the single FET gate bias, $V_{\rm ref}$ with multiple gate biases $(V_{{\rm bias}_N-1}, V_{{\rm bias}_N-2}, \ldots, V_{{\rm bias}_1}, V_{{\rm bias}_0})$, with $N$ transistors all sized at $W/L$ instead of $2^N - 1$ transistors. Then, the drain currents for the $N$-bit DAC become $i_n = K(W/L)(V_{{\rm bias}_n} - V_t)^2$. This new technique is referred to as the *multibias* DAC, because each DAC branch uses an independent FET gate bias. Hence, relative currents are controlled by gate bias rather than by geometry. This permits each branch to use identically sized devices, which is the key to area reduction while preserving device tracking, as shown in Fig. 1(a) for an 8-bit DAC. The biases are generated using currents drawn through diode connected FETs with the aid of a conventional binary-weighted DAC, as shown in Fig. 1(b). Although this second DAC would appear to impart a high area penalty, it is instantiated only once per chip to service a much larger array of reduced area stimulus circuits based on the multibias concept. The bias voltages $V_{{\rm bias}_N-1}$–$V_{{\rm bias}_0}$ are, therefore, generated centrally and distributed to all of the DACs throughout the stimulator.

## III. Circuit Implementation

### A. Architecture

The architecture of the prototype chip for the proposed stimulus circuit is shown in Fig. 2. It is programmed serially using digital *clock* and *data* input pins. The chip processes a *configuration* packet and a *stimulus* data packet. Digital data is shifted into a 15-bit first-in-first-out (FIFO) shift register $Q_{14}$–$Q_0$ on each *clock* cycle and is then latched into either a 15-bit *configuration* data register using the *load-config* input or else into an 11-bit *stimulus* data register using the *load-DAC* input. Bits $R_5$–$R_0$ tune the adjustable resistance in the current reference circuit (or select an off-chip $R_{\rm bias}$ using $R_E$), bits $G_3$-$G_0$ program the current gain prescalar (discussed in Section III-E1), bits $O_4$-$O_0$ program the multibias dc-offset DAC (discussed in Section III-E2), and bits $D_7$-$D_0$ of the stimulus data register program the 8-bit multibias stimulus DAC (discussed in Section III-B). The current outputs from the stimulus DAC and the dc-offset DAC are summed and passed into the biphasic current output amplifier. Bits $A$ and $C$ determine current steering within

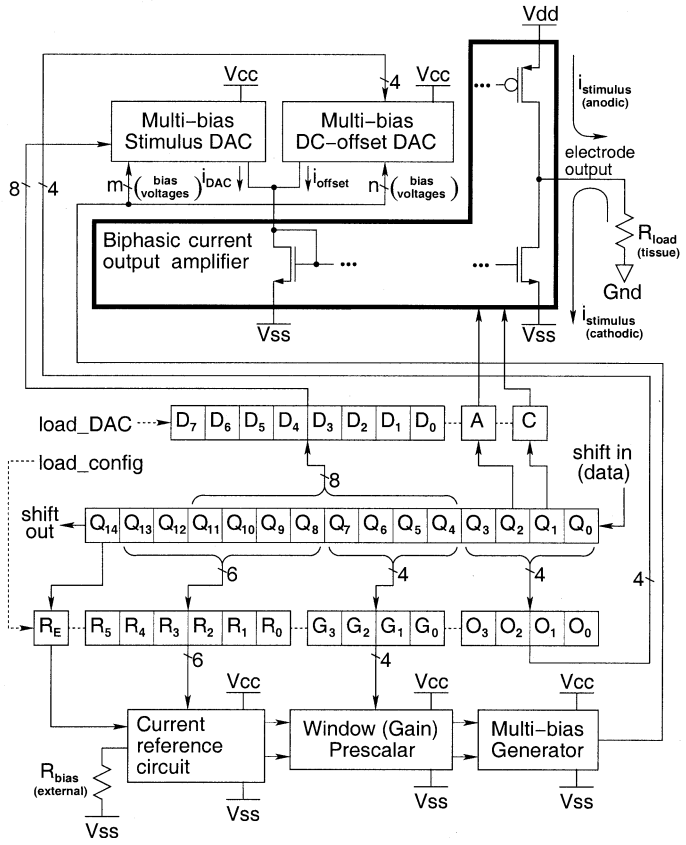


Fig. 2. System block diagram for the reduced-area (multibias) DAC prototype chip.

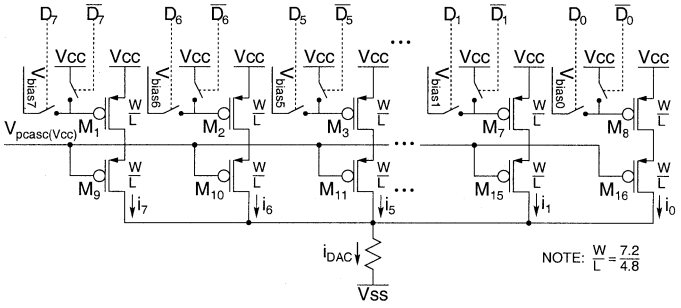


Fig. 3. Wide-swing cascoded configuration of the multibias DAC.

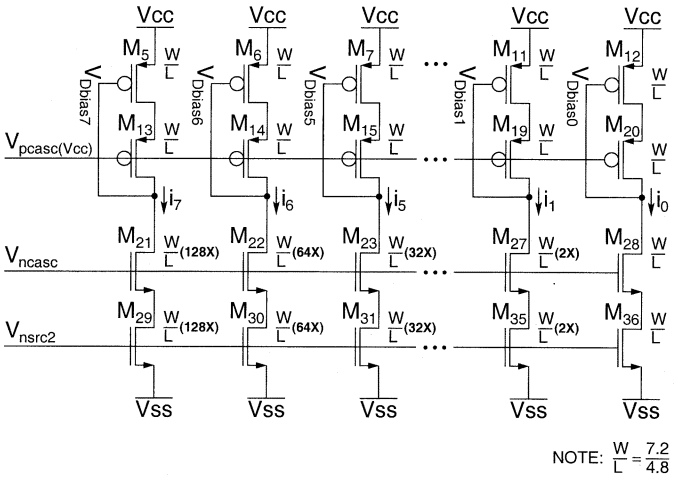


Fig. 4. Wide-swing cascoded 8-bit multibias generator (biases shown for the stimulus DAC only).

the output amplifier (discussed in Section III-D), to produce either an anodic or cathodic current pulse.

### *B. 8-Bit Wide-Swing Cascoded Multibias DAC*

INL and DNL in the transfer characteristic of the multibias DAC are sensitive to correctly scaled currents in the DAC branches. Each branch current $i_k$ associated with a digital input bit $D_k$ should be twice the magnitude of branch current $i_{k-1}$. Therefore, we have investigated the performance of a wide-swing cascoded form of the multibias DAC, as shown in Fig. 3. This structure provides increased output impedance for improved branch current tracking, while requiring only one additional cascode bias to be distributed to the DACs.

### *C. Multibias Generator*

The multibias generator, shown in Fig. 4, is a centrally located circuit which produces gate bias potentials for all the multibias DACs. It is analogous to Fig. 1(b) with the exception that the devices are now wide-swing cascoded. The bias voltages of $V_{\mathrm{ncasc}}$ and $V_{\mathrm{pcasc(Vcc)}}$, as well as $V_{\mathrm{pcasc(Vdd)}}$ from Fig. 5, are produced in a tunable current reference circuit based on the type from our prior stimulator IC design [10], with the addition of a digitally adjustable biasing resistance to

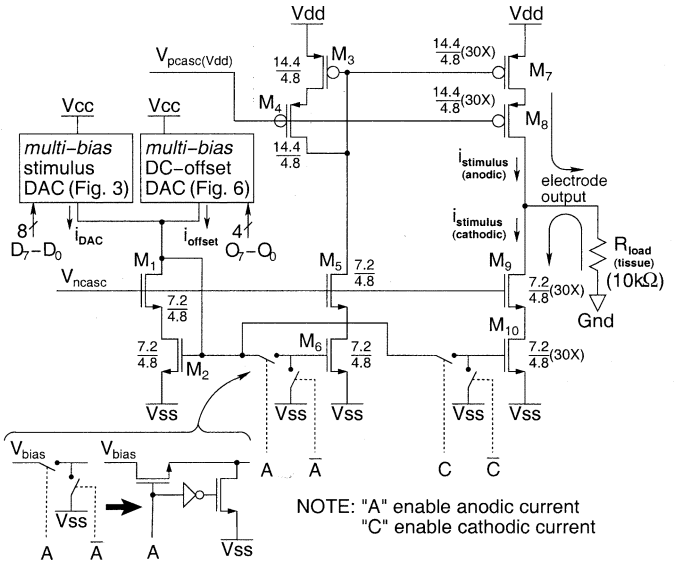


Fig. 5. Biphasic current output amplifier.

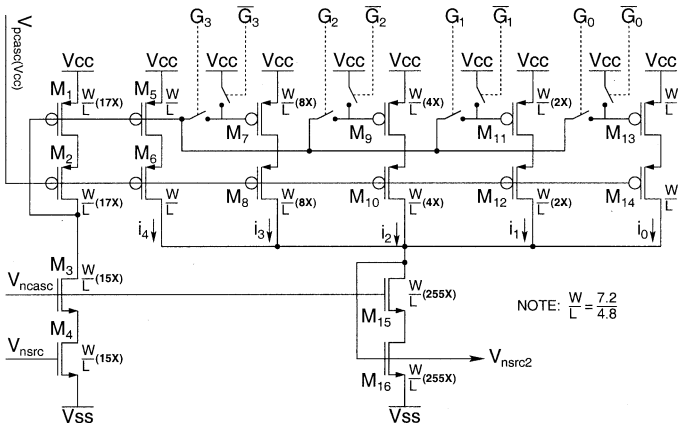


Fig. 6. Digitally programmable 4-bit reference-current gain prescalar circuit.

tune the reference current. The bias voltage of $V_{\rm nsrc2}$ derives from the gain prescalar from Fig. 6, which in turns uses $V_{\rm nsrc}$ from the current reference circuit. NFETs $M_{21}$–$M_{28}$ and $M_{29}$–$M_{36}$ in Fig. 4 form the wide-swing cascoded weighted DAC which mirrors this reference current in binary-weighted fractional increments. The resulting current-source bias potentials $V_{\rm Dbias7}, V_{\rm Dbias6}, \ldots, V_{\rm Dbias0}$ along with the cascode bias $V_{\rm pcasc(Vcc)}$ form the set of biases which are distributed to the multibias stimulus DACs.

### D. Biphasic Output Current Amplifier

The current $i_{\rm DAC}$ from the multibias DAC is passed into a biphasic current amplifier, which acts as an output stage to drive the tissue impedance. It is detailed in Fig. 5. The current from the DAC is passed into NFETs $M_1$ and $M_2$, which form the reference branch of a wide swing cascode mirror formed with $M_5$ and $M_6$ (for producing the anodic pulse) and with $M_9$ and $M_{10}$ (for producing the cathodic pulse). Output stage FETs $M_7, M_8, M_9$, and $M_{10}$ are 30 times wider in order to mirror the multibias DAC up to full-scale level of 400 $\mu$A [4]. Logic signals $A, \bar{A}$ and $C, \bar{C}$ control complementary switches to enable or disable the anodic ($M_3$–$M_8$) and cathodic currents $(M_9, M_{10})$ currents, respectively. As this output stage is intended for our epi-retinal prosthesis [10], the combined electrode/retina impedance is modeled with the load resistance $R_{\rm LOAD}$. Although the value of this load varies with geometry of the electrode, extent of retinal degeneration, and frequency of stimulation, impedances on the order of 10 k$\Omega$ have be observed experimentally [3]. Wide-swing cascode current mirrors are used in the output stage to achieve maximum output current per supply voltage while maintaining FET operation in the saturation region [12].

### E. Gain/Offset Scaling of Stimulus Currents

Generally, more advanced retinal degradation is accompanied by a greater stimulation threshold requiring a minimum current $i_{\rm threshold}$ to elicit perception. Moreover, sensitivity in perception to brightness variation should saturate at some current amplitude $i_{\rm saturation}$ with no change in perception from increased stimulus currents. The prototype IC implements a gain prescalar and a dc-offset DAC which produce a current *gain* and *offset* to define $i_{\rm threshold}$ and $i_{\rm saturation}$. These establish the operating range of the the 8-bit multibias DAC such that $i_{\rm threshold} \leq i_{\rm stimulus} \leq i_{\rm saturation}$ from the output amplifier. This prevents the loss of stimulus resolution over the domain of excitation currents which are effective for eliciting perception, and thus, provides greater flexibility for device optimization compared with our previous IC design [10].

*1) Programmable Current Gain Prescalar:* The gain prescalar circuit, shown in Fig. 6, allows the master reference current to be scaled from 1/16th to 100% of its nominal value with 4-bit linear resolution. A copy of the reference current is reproduced from biases $V_{\rm ncasc}$ and $V_{\rm nsrc}$ in NFETs $M_3$ and $M_4$, which is passed to the wide-swing cascoded reference branch of $M_1$ and $M_2$. This current is fractionally mirrored into the binary-weighted branches of $M_5$–$M_{14}$, thus implementing a 4-bit conventional wide-swing cascoded current-mode DAC. The complementary switches controlled by $G_3$–$G_0$ enable the DAC branches by switching the gate potential of the current source PFETs ($M_7, M_9, M_{11}$, and $M_{13}$) to either the bias voltage from the reference branch (ON state) or to $V_{\rm dd}$ (OFF state). The unswitched branch of $M_5$ and $M_6$ prevents a gain of zero such that $G_3$–$G_0 = 0000$ does not yield zero current. Selected current from the prescalar DAC is passed to NFETs $M_{15}$ and $M_{16}$ and then mirrored into the multibias generator, to supply bias potentials for the stimulus DACs. The prescalar current programmed by $G_3$–$G_0$ establishes a full-scale current over which the multibias DAC exercises its 8-bit resolution using bits $D_7$–$D_0$. The gain prescalar is implemented only once on the chip to establish a global shared current gain for all of the multibias stimulus circuits on chip.

*2) Programmable Multibias DC-Offset DAC:* The offset DAC, shown in Fig. 7, provides the minimum current of $i_{\rm threshold}$ by implementing a 4-bit current-mode DAC which again scales the master reference current from zero to its nominal value. The dc-offset DAC is contained in each stimulus circuit. Accordingly, it is implemented using the proposed multibias concept to reduce area. Accordingly, it taps gate bias voltages from the central multibias generator.

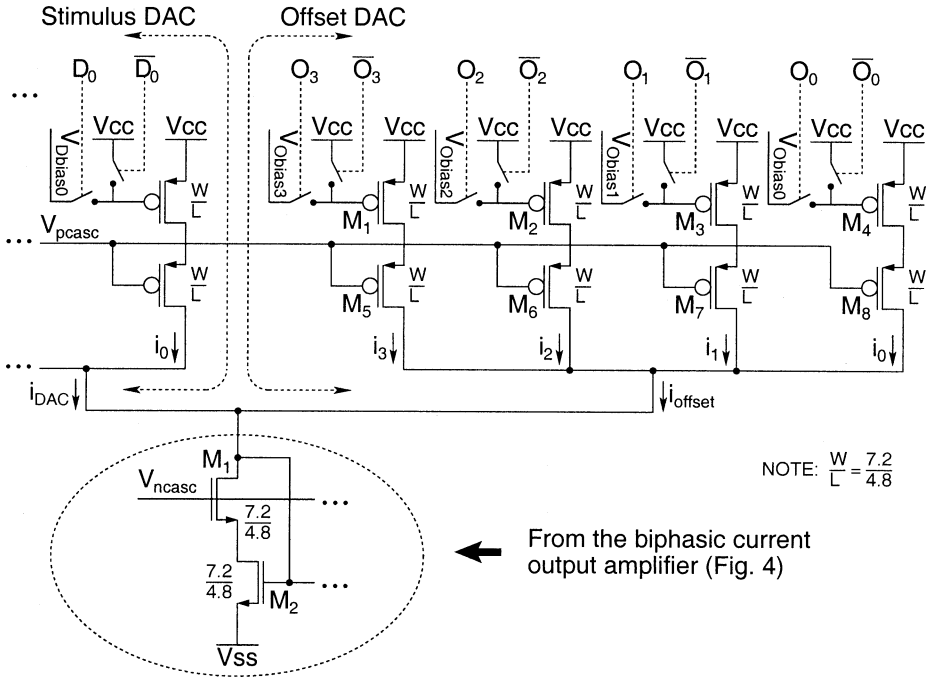


Fig. 7. Digitally programmable 4-bit multibias dc-offset DAC (in parallel with the 8-bit multibias stimulus DAC).

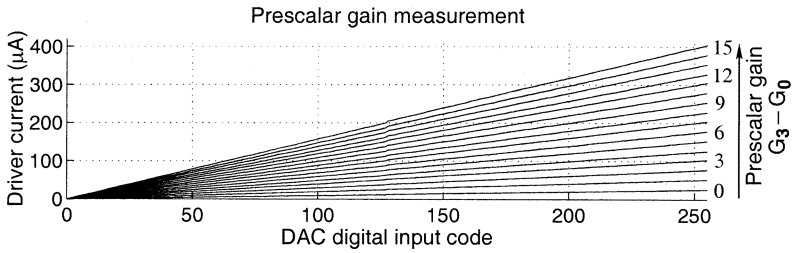


Fig. 8. Experimental measurement of the 4-bit gain prescalar.

The DAC is implemented with PFETs $M_1$–$M_8$ equally sized, which implement wide-swing cascoded current mirrors in the same manner as in the multibias stimulus DAC. Bits $O_3$–$O_0$ control complementary switches to enable or disable the DAC branches. The selected current is connected in parallel with the current from the 8-bit multibias stimulus DAC, summing the two currents into the load (recall from Fig. 5).

## IV. Measured Results

The prototype chip was fabricated in 1.2-$\mu$m CMOS with a die size of 2.2 mm $\times$ 2.2 mm. Measurements are taken of the circuit's output current delivered to the load resistance, $R_{\mathrm{LOAD}} = 10$ k$\Omega$, as shown in Fig. 5. An important design criteria in circuits for bioimplantable neurostimulators is that biphasic currents be charge balanced in order to protect the electrodes. Therefore, the performance of the new multibias DAC in Fig. 3 and the output amplifier of Fig. 5 is characterized in terms of linearity, and accuracy (or tracking). Power-supply sensitivity is measured due to anticipated transient disruptions in supply levels if powered from a wireless telemetry link where relative motion between coils can occur. Power consumption and output impedance are also assessed.

### A. Gain Prescalar Measurement

In measuring the performance of the gain prescalar, the current reference circuit is tuned to yield $i_{\mathrm{stimulus}}$ of 400 $\mu$A. Sixteen separate measurements were taken, one for each setting of the 4-bit prescalar circuit. For each gain setting, the digital input to the 8-bit multibias stimulus DAC was swept from 00(hex) to FF(hex). This produces a stimulus current $i_{\mathrm{stimulus}}$ in $R_{\mathrm{load}}$ ranging from zero to the maximum value determined by prescalar current $(\times 30)$, with a full-scale expected anodic and cathodic current of 400 $\mu$A. The dc-offset DAC of Fig. 7 was set to $O_3$–$O_0 = 0000$ during these measurements. The experimental measurements overlayed and shown in Fig. 8 indicate that the gain prescalar can effectively vary the full-scale $i_{\mathrm{saturation}}$ value.

### B. DC-Offset Measurement

In measuring the performance of the dc-offset DAC, sixteen separate measurements are again taken for each selectable offset level. For each setting, the digital input to the 8-bit multibias stimulus DAC is swept from 00(hex) to FF(hex). This yields a stimulation current $i_{\mathrm{stimulus}}$ in $R_{\mathrm{load}}$ ranging from a minimum value established by the dc-offset DAC $(\times 30)$ to a maximum value determined by the prescalar current $(\times 30)$, with

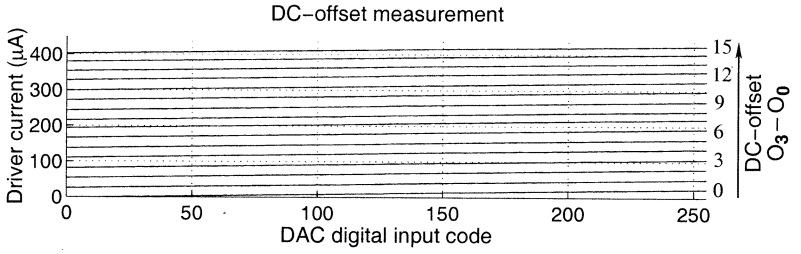


Fig. 9. Experimental measurement of the multibias dc-offset DAC.

a full-scale expected anodic and cathodic current of 400 $\mu$A. At $V_{\rm dd}/V_{\rm ss} = \pm 5$ V load current much beyond 400 $\mu$A will force PFETs $M_7$–$M_{10}$ of the biphasic amplifier into the linear region and will clip the output current. This is evident in the curves of Fig. 9, where the gain prescalar is programmed at a setting of $\langle G_3 \colon G_0 \rangle = 1000$ (binary), corresponding to a full-scale load current of approximately 260 $\mu$A. For this setting, a dc-offset programmed setting near $\langle O_3 \colon O_0 \rangle = 0111$ (binary) and beyond will lead to clipping. In practice, the gain prescalar and offset DAC would together be programmed to implement $i_{\rm threshold}$ and $i_{\rm saturation}$ current limits within the drive capabilities of the stimulus circuits. The experimental measurements shown in Fig. 9 indicated that the multibias dc-offset DAC wired in parallel with the stimulus DAC can effectively establish $i_{\rm theshold}$ to conserve resolution in the stimulus DAC.

### C. Linearity

Linearity in the DAC's transfer characteristic is useful for characterizing the effectiveness of tissue stimulation as a function of current amplitude. Thus, we measure the INL and DNL errors in the currents delivered to $R_{\rm LOAD}$. INL is measured with respect to a straight line connecting the endpoints. That is, $\mathrm{INL}(n) = (i(n) - n\Delta_{\rm LSB} + i(0)/\Delta_{\rm LSB})$, for $0 \le n < 2^N$ where $\Delta_{\rm LSB} = (i(2^N - 1) - i(0)/2^N)$, for $N = 8$ bits. DNL is measured as the ratio of the actual step size to the nominal step size. That is, $\mathrm{DNL}_{(n)} = (i(n+1) - i_{(n)}/\Delta_{\rm LSB})$, for $0 \le n < 2^N$. Accordingly, the error in the anodic and cathodic currents is shown in Fig. 10(a) and (b). Maximum error is $-3.11$ LSB and 1.59 LSB, respectively. The DNL error in the anodic and cathodic currents is shown in Fig. 10(c) and (d), for which maximum errors are 2.15 LSB and 2.11 LSB, respectively. This renders the 8-bit DAC to six bits of accuracy. Circuit simulations show that the multibias DAC concept is susceptible to DNL errors. We discovered that the reference currents in FETs $M_5$–$M_{20}$ in the multibias generator (Fig. 4) and the mirrored currents in FETs $M_1$–$M_{16}$ of the multibias DAC (Fig. 3) did not match precisely, but were instead mirrored to the DAC with positive offsets which became progressively larger for the higher order bits. The source of these offsets is related to the difference in output impedance between FETs $M_5$–$M_{20}$ in the multibias generator and FETs $M_1$ and $M_2$ in biphasic amplifier into which the multibias DAC delivers its current $i_{\rm DAC}$. As the widths of $M_5$–$M_{20}$ increase from $(W/L)(1\times)$ to $(W/L)(128\times)$, the discrepancy in mirrored current increases. When stepping through the DAC digital input in a binary fashion, these current offsets lead to negative DNL errors at each major bit transition $(\ldots 00000111 \rightarrow 00001000, 00001111 \rightarrow 00010000, \ldots, 01111111 \rightarrow 10000000)$. In order to achieve these measurements in spite of the inherent nonmonotonicty in the wide-swing form of the multibias DAC, it was necessary to increase the widths of $M_6$ and $M_{14}$ to $2W/L$ and $M_5$ and $M_{13}$ to $4W/L$ in the multibias generator (Fig. 4) with identical changes to $M_2, M_{10}, M_1$, and $M_9$ in the multibias DAC (Fig. 3). This is estimated to increase the implementation area by approximately 10% of the what it otherwise would be if all FETs were sized at $W/L$.

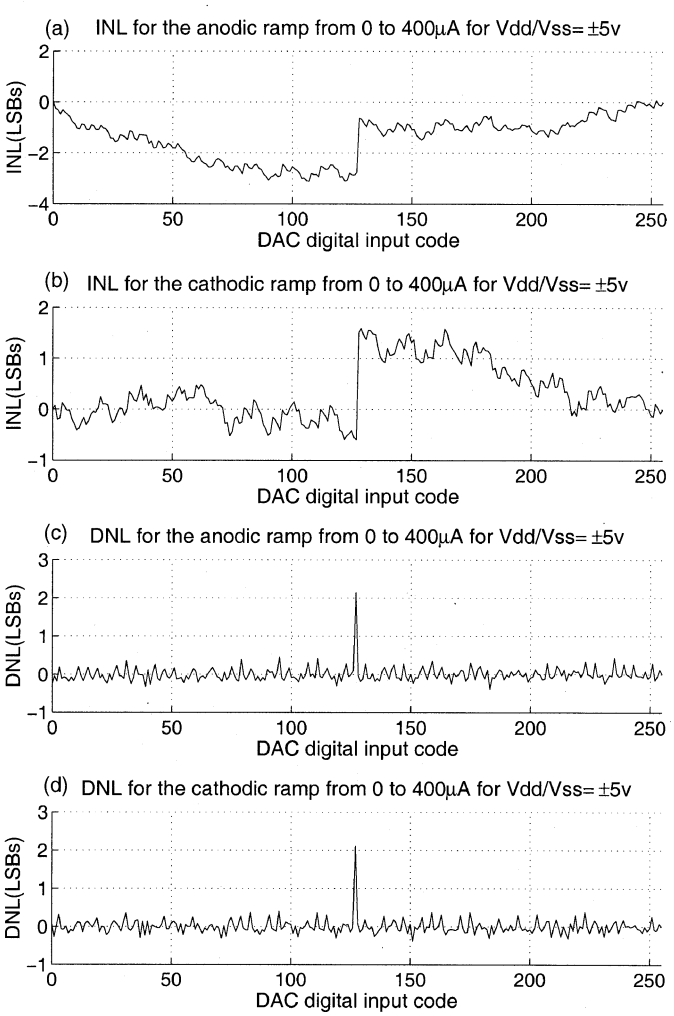


Fig. 10. Experimentally measured integral and differential nonlinearity characteristics of current outputs from Fig. 5 at 400-$\mu$A full-scale current.

Although not fabricated on the test chip, we subsequently discovered that a fully cascoded form of the multibias generator and DAC, shown in Fig. 11, is more immune to these

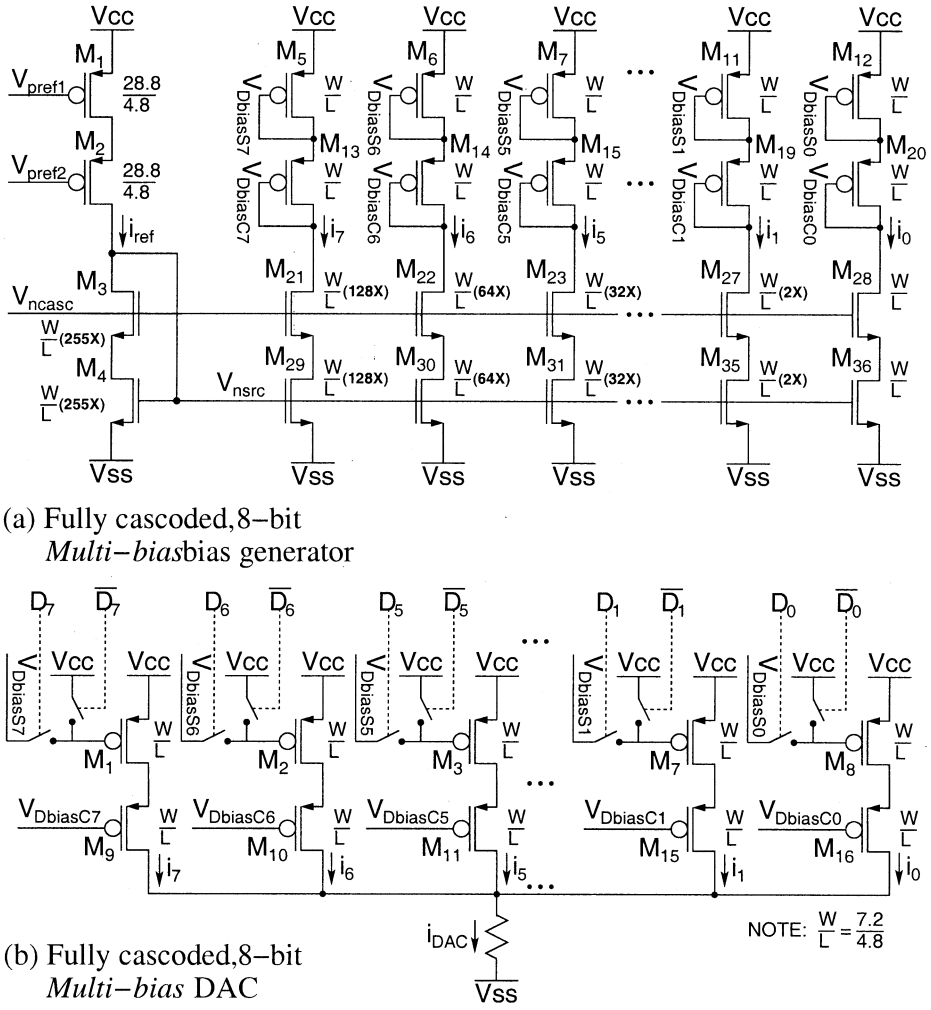


Fig. 11. Fully cascoded topology of the multibias concept.

nonmonotonicities because of the higher output impedance of this circuit structure. It, therefore, produces negligible offsets in the mirrored currents yielding improved INL and DNL without the need to extend device sized in the high order bits. Circuit simulation yields curves similar to those in Fig. 10 with lower maximum INL errors of 1.31 LSB and 0.45 LSB for the anodic and cathodic currents, respectively, and reduced maximum DNL errors of $-0.55$ LSB for both currents. This improvement in INL and DNL comes at the expense of a greater number of bias potentials which must be distributed to the DACs (eight current source biases plus eight cascode biases, for a total of 16 per DAC for 8-bit resolution).

### D. Accuracy

We measure the accuracy in terms of the tracking between the anodic and cathodic currents. Fig. 12 provides the current amplitude of the two currents delivered into $R_{\rm LOAD}$ for a full-scale $i_{\rm stimulus}$ value of 400 $\mu$A at $V_{\rm dd}/V_{\rm ss} = \pm 5.5$ V. The increase of $V_{\rm dd}/V_{\rm ss}$ to $\pm 5.5$ V was determined experimentally to keep the pMOS mirrors from entering the linear region. The measurement shows that the anodic current is less by an amount equal to 14.56 LSB at $D_7$–$D_0 = {\rm FF}_{16}$ or 5.74% with respect to the cathodic current. The charge imbalance on electrodes due to this mismatch could be depleted with a charge cancellation or shorting circuit in the output stage briefly connecting $R_{\rm LOAD}$ to the ground return potential [10].

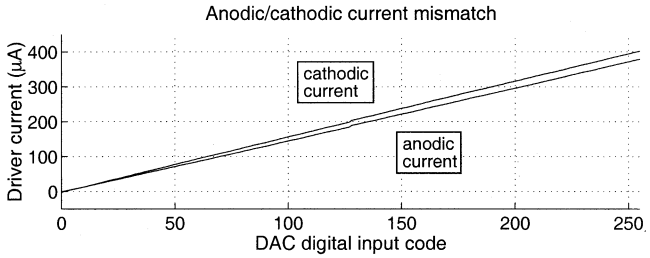


Fig. 12. Experimentally measured current amplitude matching between the anodic and cathodic phases for 400-$\mu$A full-scale current.

### E. Power-Supply Sensitivity

When a neurostimulator is powered inductively, relative movement between exterior and interior coils will cause a modulation of the dc supplies to the chip. To characterize the sensitivity to this, we measured the anodic and cathodic currents $i_{\rm stimulus}$ for $5\ {\rm V} \le V_{\rm dd} \le 7\ {\rm V}$ and $-7\ {\rm V} \le V_{\rm ss} \le -5\ {\rm V}$. Results in Fig. 13 show good supply immunity for full-scale current amplitudes in $i_{\rm stimulus}$ of 200 and 400 $\mu$A, with 2.5 ($\mu$A/V) measured for the 400-$\mu$A anodic current.

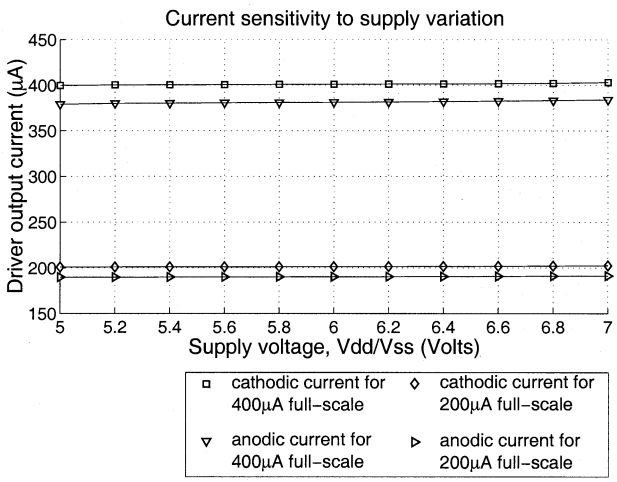


Fig. 13. Experimentally measured current dependence on supply variation.

### F. Power Consumption

The multibias DAC claims to provide area improvements over the conventional binary-weighted DAC. Therefore, power consumptions associated with these two topologies are compared. Unfortunately, the binary-weighted DAC was not fabricated on our prototype chip. Furthermore, the circuits stages do not use isolated power-supply pins which would facilitate the analysis of an experimental measurement of the power consumption to be made on the prototype chip. Therefore, we have used circuit simulation for comparison of the power consumption of these two DAC structures. A sequence of 100 biphasic pulses of random amplitude at 100-Hz repetition rate was instructed, in which the anodic and cathodic amplitudes were equal and pulse widths were 2 ms. Full-scale current was 400 $\mu$A. By generating such a sequence in this way, the effect of switching the gate capacitances was included. Over the duration of this sequence, the binary weighted yields an average power of 26.70 $\mu$W while the multibias DAC yields a slight improvement of 26.67 $\mu$W. This difference is accounted for by the reduced gate capacitance of the multibias DAC. The biphasic output stage itself is the same in both cases and has an average power consumption of 217.32 $\mu$W for a total of 244 $\mu$W.

### G. Output Impedance

The current output of the multibias DAC on the prototype chip is not accessible off chip, but instead passes directly into the biphasic output stage. Therefore, we have used circuit simulation to assess the output impedance, voltage swing, and current limitations of the variations in multibias DAC topology. The $I$–$V$ characteristic of the wide-swing cascoded topology which was implemented on the prototype chip is shown in Fig. 14 when biased to several values of current. The bold curve represents the $I$–$V$ trajectory followed by the DAC as it proceeds from a 00(hex) to FF(hex) with a full-scale current of 13.33 $\mu$A, which gives the targeted 400-$\mu$A stimulus current after $30\times$ gain in the output stage. An output impedance of 16.45 M$\Omega$ was determined at 13.33 $\mu$A, which remains greater than 16 M$\Omega$ for a voltage headroom as low as 2.46 V.

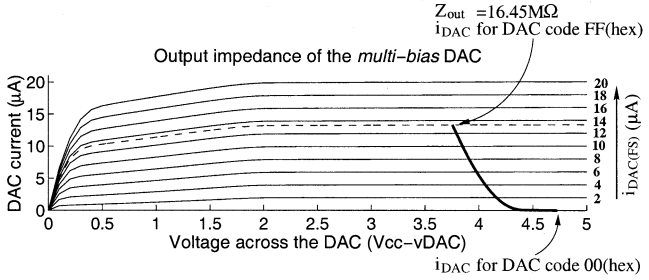


Fig. 14. Circuit simulation of the output impedance of the wide-swing cascoded multibias DAC as implemented on the prototype chip.

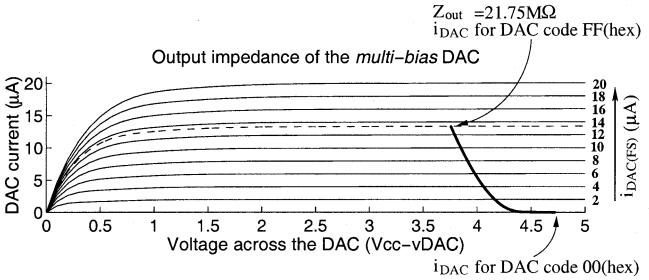


Fig. 15. Circuit simulation of the output impedance of the fully cascoded multibias DAC proposed as a design enhancement.

The family of $I$–$V$ curves for the fully cascoded implementation is shown in Fig. 15. These curves indicate a higher output impedance of 21.76 M$\Omega$ at 13.33 $\mu$A, which remains greater than 20 M$\Omega$ for a voltage headroom as low as 2.48 V.

The wide-swing cascoded topology is expected to allow for a lower voltage headroom while allowing the devices to remain in saturation. This was not evident by comparing Figs. 14 and 15 where both topologies appear to have approximately the same minimum headroom of about 2.5 V. We determined that the wide-swing cascoded topology is not optimally biased from a single cascode bias potential, *ws_pbias*. Instead, each of the eight branches of the multibias generator needs an independent cascode bias *ws_pbias*$_i$ for $7 \geq i \geq 0$. In this case, the minimum allowable headroom for the DAC decreases to about 1 V. The output impedance at 13.33 $\mu$A is 9.22 M$\Omega$ and remains greater than 4.26 M$\Omega$ down to 1 V. This additional requirement of independent cascode biases defeats the sole advantage of the wide-swing cascoded topology, which was to reduce the number of bias potentials needed to use large numbers of multibias DAC on stimulator ICs. The reduced headroom accompanying a wide-swing topology is not really necessary since the current level is so low (13.33 $\mu$A) in lieu of the $30\times$ gain in the output stage. Ultimately, the fully cascoded topology becomes the best choice for the multibias DAC since its high output impedance most effectively minimizes nonmonotonicities in the DAC staircase transfer function. Both the wide-swing cascoded (as implemented) and the fully cascoded topologies provide up to 36 $\mu$A of current while remaining in saturation. Accordingly, when sourcing the nominal full-scale current of 13.33 $\mu$A, the preferred fully cascoded implementation would have about 1 V of additional headroom.

A graph of the experimental measurement of anodic and cathodic stimulus current amplitude versus the voltage across the

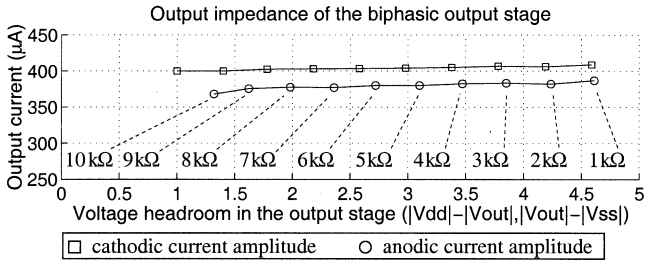


Fig. 16. Experimental measurement of the output impedance of the biphasic output amplifier stage.

biphasic output stage is shown in Fig. 16. Each point corresponds to a unique resistive load applied to the circuit. From a least squares linear fit to this data, the output impedance of the anodic (pMOS) and cathodic (nMOS) circuitry of the output stage was determined to be 236 and 443 kΩ, respectively. This is lower than would be desired for a current source. The slope of the $I_{\rm DS}$ versus $V_{\rm DS}$ curves in the saturation region (owing to channel length modulation) increases for progressively higher values of $V_{\rm GS}$ (i.e., the biased drain current). In these measurements, the circuits are biased to deliver the maximum nominal stimulus current of 400 $\mu$A, which yields a much lower output impedance than would be encountered at lower current levels. The output impedance could be improved by replacing the wide-swing cascoded output stage with a fully cascoded stage, but would require higher supply voltages and would worsen power consumption for a stimulator IC using this circuit. The impact of channel length modulation could be "softened" with longer channel devices (thereby improving the output impedance). But, unless the $W/L$ ratio is maintained by widening the devices accordingly, the voltage swing benefit of the wide-swing mirrors is compromised. Therefore, in light of the competing constraints of chip area (which the multibias DAC was designed to enhance) and of power consumption, the lower output impedance of the output stage is tolerated in the biostimulator application.

### *H. Sensitivity of Bias Voltages to Noise*

A sensitivity analysis of multibias DAC branch currents to bias noise is summarized in Table I. These branch currents correspond to $i_7$–$i_0$ as annotated on the fully cascoded multibias DAC of Fig. 11. In this study, the branch currents were simulated with ±10 mV of dc noise offset from the nominal values of the eight current-source bias potentials, $V_{\rm DbiasS7}$–$V_{\rm DbiasS0}$ of PFETs $M_5$–$M_{12}$, and the eight cascode bias potentials $V_{\rm DbiasC7}$–$V_{\rm DbiasC0}$ of PFETs $M_{13}$–$M_{20}$. As expected, the noise on biases $V_{\rm DbiasS7}$–$V_{\rm DbiasS0}$ imparts greater current disturbance than noise on biases $V_{\rm DbiasC7}$–$V_{\rm DbiasC0}$. Furthermore, the lower significant bits exhibit more sensitivity expressed in percent difference. However, in spite of a lower sensitivity to noise in the higher order bits, as the nominal currents increase by factors of two, the ±10 mV of bias noise results in a larger absolution deviation in the current. If routing resources allow, a better solution would provide grounded shielding for all sixteen bias potentials. If a compromise must be made, then shielding preference should be given to the current source biases, $V_{\rm DbiasS7}$–$V_{\rm DbiasS0}$, owing to their greater sensitivity to noise.

TABLE I
BRANCH CURRENT SENSITIVITY TO BIAS NOISE

| bias[1] | nominal value [$V_{DC}$] | nominal $i_{DS}$[2] [μA] | $\Delta i_{DS}$[3] from +10mV ΔV [nA] | % diff | $\Delta i_{DS}$[3] from −10mV ΔV [nA] | % diff |
|---|---|---|---|---|---|---|
| $V_{DbiasS7}$ | 5.188 | 10.030 | −189.43 | −1.89 | 191.00 | 1.90 |
| $V_{DbiasS6}$ | 5.473 | 5.0270 | −138.39 | −2.75 | 140.12 | 2.79 |
| $V_{DbiasS5}$ | 5.67 | 2.5220 | −100.19 | −3.97 | 102.06 | 4.05 |
| $V_{DbiasS4}$ | 5.806 | 1.2670 | −72.56 | −5.72 | 74.50 | 5.88 |
| $V_{DbiasS3}$ | 5.9 | 0.6379 | −52.76 | −8.28 | 54.82 | 8.60 |
| $V_{DbiasS2}$ | 5.965 | 0.3219 | −37.57 | −11.73 | 39.94 | 12.47 |
| $V_{DbiasS1}$ | 6.011 | 0.1628 | −25.28 | −15.61 | 27.91 | 17.24 |
| $V_{DbiasS0}$ | 6.046 | 0.0823 | −15.78 | −19.25 | 18.28 | 22.30 |
| $V_{DbiasC7}$ | 3.037 | 10.030 | −5.70 | −0.06 | 5.70 | 0.06 |
| $V_{DbiasC6}$ | 3.653 | 5.0270 | −3.86 | −0.08 | 3.84 | 0.08 |
| $V_{DbiasC5}$ | 4.078 | 2.5220 | −2.62 | −0.10 | 2.61 | 0.10 |
| $V_{DbiasC4}$ | 4.373 | 1.2670 | −1.81 | −0.14 | 1.81 | 0.14 |
| $V_{DbiasC3}$ | 4.576 | 0.6379 | −1.27 | −0.20 | 1.27 | 0.20 |
| $V_{DbiasC2}$ | 4.716 | 0.3219 | −0.89 | −0.28 | 0.89 | 0.28 |
| $V_{DbiasC1}$ | 4.816 | 0.1628 | −0.60 | −0.37 | 0.60 | 0.37 |
| $V_{DbiasC0}$ | 4.893 | 0.0823 | −0.38 | −0.46 | 0.38 | 0.46 |

[1]Bias potentials correspond to the 8-bit fully cascoded bias generator of Figure 11a set to produce a 20μA full-scale current in the multi-bias DAC of Figure 11b ("S" subscript refers to a current-source bias potential; "C" subscript refers to a cascode bias potential).
[2]Branch current is taken in association with the corresponding bias.
[3]Bias potential is offset ±10mV to model noise.

TABLE II
CHIP PERFORMANCE SPECIFICATION AND MEASUREMENTS

| | |
|---|---|
| Technology | MOSIS 1.2μm CMOS |
| Die size | 2.2mm × 2.2mm |
| Area | |
| *multi-bias* generator | 0.177 mm$^2$ |
| *multi-bias* DAC | 0.0264 mm$^2$ |
| binary current-weighted DAC | 0.107 mm$^2$ |
| biphasic output amplifier | 0.0237 mm$^2$ |
| Amplitude resolution | 8-bits |
| INL | |
| Anodic output current | -3.11 LSB |
| Cathodic output current | 1.59 LSB |
| DNL | |
| Anodic output current | 2.15 LSB |
| Cathodic output current | 2.11 LSB |
| Anodic/Cathodic mismatching | 14.56 LSB (5.74%) |
| Supply sensitivity | 2.5 μA/V |
| Power consumption | |
| *multi-bias* DAC | 26.70 μW |
| binary current-weighted DAC | 26.67 μW |
| biphasic output stage | 217.32 μW |
| Output impedance | |
| Wide-swing cascoded *multi-bias* DAC | 16.45 MΩ |
| Fully cascoded *multi-bias* DAC | 21.75 MΩ |
| PMOS half of the biphasic output stage | 236 kΩ |
| NMOS half of the biphasic output stage | 443 kΩ |

### *I. Area Reduction*

A summary of the experimental measurements and simulations results is provided in Table II. A die photograph of the prototype chip is shown in Fig. 17. The die measures 2.2 mm × 2.2 mm and was fabricated in the AMI 1.2-$\mu$m CMOS process through MOSIS. The area occupied on the chip by the 8-bit multibias generator is 0.177 mm$^2$, which while appearing significant is incurred only once per chip to service an array of multibias DACs. The binary-weighted DAC employed within the multibias generator occupies an area of 0.107 mm$^2$. The multibias DAC, on the other hand, consumes 0.0265 mm$^2$, for a savings of 75% compared with the conventional binary current-weighted DAC, with potentially higher savings from tighter layout in more advanced IC processes having more than two metal layers for routing the bias potentials, as was available in AMI 1.2-$\mu$m CMOS. In AMI 1.2-$\mu$m CMOS, the

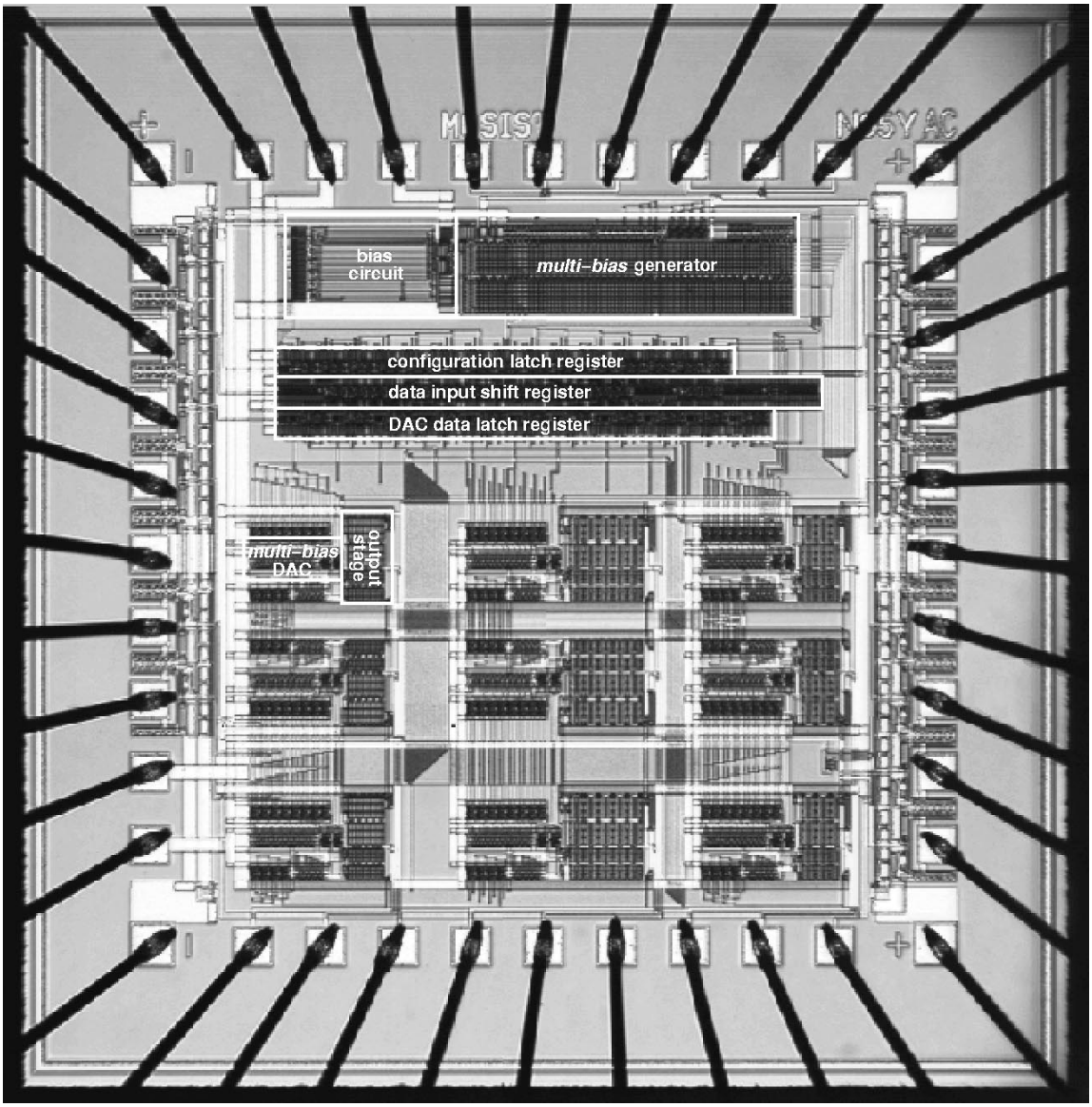


Fig. 17. Die micrograph of the *multibias* DAC prototype IC.

fully cascoded multibias DAC topology is estimated to require about 25% more area that the wide-swing cascoded topology, owing to the routing overhead of the additional bias potentials.

## V. Improvements and Design Enhancements

One concern of the multibias concept to reduce area regards the impact of noise on the bias voltages. Future implant ICs will contain arrays of hundreds of stimulator circuits, with the bias potentials of the multibias DACs distributed across the chip from the central multibias generator. Two foreseeable sources of noise exist. Our recent stimulator devices [10] are mixed-signal designs with digital clocks and data distributed throughout the chip alongside analog dc bias potentials with capacitively coupled noise. In the AMI 1.2-$\mu$m process with its two metal layers, there is limited routability to protect the bias potentials from noise on adjacent interconnect and from noise injected into the substrate. In more advanced IC processes with more metal layers, all of the multibias potentials can be collected into a common group with grounded interconnect on either side of the group and grounded metal shield planes above and below the group [15]. However, when the complementary switches in the multibias DACs toggle state, clock feedthrough noise can couple onto the multibias interconnect and affect other multibias DACs sharing those biases. Replacing these switches with single FET pass gates in series with the branch current will remove clock feedthrough noise onto the bias voltages, albeit at the cost of higher $V_{cc}$ necessary to keep the DAC FETs saturated. In this configuration, the unswitched bias potentials connect directly to the FET gate terminals and provide additional noise immunity in that the biases are "buffered" by the combined gate capacitances of all the multibias DACs. Noise associated with series switching of the branch current should not be problematic as it relates to electrical stimulation in our retinal prosthesis. Since the time scale of this noise is much shorter than the stimulus pulse

widths needed for ganglion cell excitation [5], [16] and is shorter than the refractory times of the neurons/cells [17], it is not expected to elicit perceptual artifacts.

## VI. Conclusion

We have introduced key improvements to the stimulus circuit used in our existing retinal stimulator designs. The gain prescalar and dc-offset circuits allowed the stimulus circuits to be tuned to compensate for variations in retinal degradation per patient. In additional, a novel modification to the conventional binary-weighted current-mode DAC based on distributed multiple bias potentials was presented to significantly reduce implementation area. Measured INL and DNL of $-3.11$ and 2.15, respectively, were obtained with even better metrics expected from the fully cascoded topology. Anodic and cathodic current tracking within 5.74% was experimentally measured with good supply insensitivity of $2.5(\mu\text{A}/\text{V})$ recorded. The multibias approach significantly decreases the circuit area compared with the conventional DAC structure, resulting in a linear instead of exponential increase in area versus resolution. Transistor counts are reduced from $2(2^N-1)$ FETs for an $N$-bit conventional binary-weighted DAC using cascoded mirrors to $2N$ FETs for the reduced-area multibias DAC. Area savings for an 8-bit DAC are approximately 75%. The benefits of reduced area will be beneficial for increasing spatial resolution in stimulator devices and, consequently, the effectiveness of visual prostheses.

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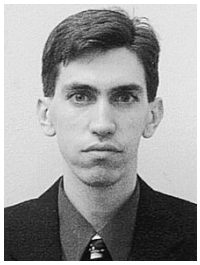

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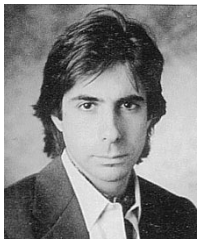

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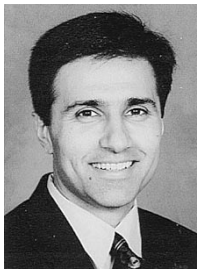

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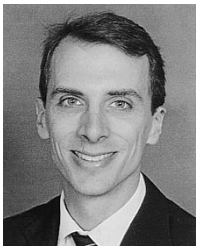

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