A Compact Large Voltage-Compliance High Output-Impedance Programmable Current Source for Implantable Microstimulators

Maysam Ghovanloo*, *Member, IEEE* and Khalil Najafi, *Fellow, IEEE*

***Abstract*—A new CMOS current source is described for biomedical implantable microstimulator applications, which utilizes MOS transistors in deep triode region as linearized voltage controlled resistors (VCR). The VCR current source achieves large voltage compliance, up to 97% of the supply voltage, while maintaining high output impedance in the 100 MΩ range to keep the stimulus current constant within 1% of the desired value irrespective of the site and tissue impedances. This approach improves stimulation efficiency, extends power supply lifetime, and saves chip area especially when the stimulation current level is high in the milliampere range. A prototype 4-channel microstimulator chip is fabricated in the AMI 1.5-μm, 2-metal, 2-poly, n-well standard CMOS process. With a 5-V supply, each stimulating site driver provides at least 4.25-V compliance and >10 MΩ output impedance, while sinking up to 210 μA, and occupies 0.05 mm^2 in chip area. A modular 32-site wireless neural stimulation microsystem, utilizing the VCR current source, is under development.**

***Index Terms*—Charge balancing, CMOS, cochlear implant, current source, implantable microelectronics, microstimulation, neural prosthesis, triode region, voltage compliance.**

I. Introduction

IMPLANTABLE microstimulators such as pacemakers, implantable cardioverter defibrillators (ICD), cochlear implants, deep brain, spinal cord, and neuromuscular stimulators [1]–[6] have found a variety of applications in treatment of various ailments. Broad research is underway to provide new devices for other applications such as visual prostheses, pain management systems, essential tremor, and bladder controllers [7]–[16]. Reducing the size and power consumption, either from an internal battery or an external transcutaneous wireless link, have been the two major challenges in designing these implantable circuits to make them less invasive and more durable. In an implantable microstimulator, the goal is to pass electric charge in a precisely controlled fashion through the excitable tissue to initiate action potentials. Part of the power out of the stimulator energy source produces the useful voltage across the stimulating electrodes and the stimulus current passing through the tissue. The rest of the power, however, is dissipated as heat in the microstimulator circuitry and should be minimized in order to improve the stimulation efficiency and limit the temperature rise within the implant.

Usually the duration and frequency of stimulus pulses and their voltage (current) amplitude are controlled by the stimulating circuitry and their current (voltage) is defined by the sum of stimulating sites and tissue impedances. Since the site and tissue impedances are highly variable, current-controlled stimulation provides more manipulation over the injected charge, and more closely mimics the natural process of tissue stimulation. So far, current-controlled stimulation is adopted where the stimulus thresholds are lower (<1 mA) such as in cochlear or retinal implants [4], [5], [9]–[12], [15], [16]. In high-current stimulators such as pacemakers and deep brain/spinal cord stimulators, however, voltage-controlled stimulation is favored, mostly because of achieving higher efficiency in stimulating with voltages closer to the supply level, leading to longer battery lifetime [1]–[3]. When the site and tissue impedances are high, conventional current sources often saturate at high currents and fail to achieve large enough voltage compliance, especially at low supply voltages when the implant battery is exhausted. In addition, despite implementation of various techniques to shrink the circuit size, typical current sources need to be made very large to handle high stimulation currents with low dropout voltage, such that they occupy most of the stimulating chip area when the number of stimulating channels is high [12].

In this paper, a new CMOS current source is proposed for biomedical implantable microstimulators, which utilizes MOS transistors in deep triode region as linearized voltage controlled resistors (VCR) in order to achieve large voltage compliance very close to the supply voltage [17]. The new current source, hereafter called the VCR current source, also maintains high output impedance to keep the desired stimulus current constant irrespective of the site and tissue impedances. This approach also saves significant chip area especially when the stimulus current is high in the milliampere range. In Section II, the basic topology and theory behind the operation of the VCR current source is described. The complete VCR stimulation circuit implementation is discussed in Section III along with simulation results. Measured experimental performance of the VCR current source in a prototype chip is reported in Section IV, followed by the concluding remarks in Section V.

II. Basic Theory and Topology

A. Existing Stimulation Circuits

Current mirrors replicating and scaling the output currents of binary-weighted current-mode digital-to-analog converters

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*M. Ghovanloo is with the Bionics Laboratory, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695-7914 USA (e-mail: mghovan@ncsu.edu).

K. Najafi is with the Center for Wireless Integrated Microsystems, University of Michigan, Ann Arbor, MI 48109-2122 USA.

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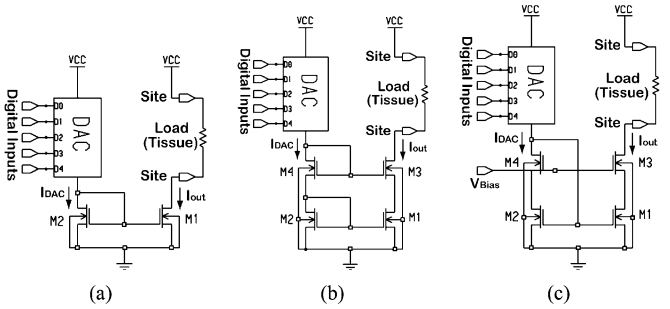

Fig. 1. (a) Simple current mirror, (b) FC current mirror, and (c) WSC current mirror, all controlled by current mode DACs, have been typically used for microstimulation with current [4], [5], [9]–[14].

(DACs) have been widely used for microstimulation circuits because of their straightforward design, linearity, and little need for decoding the digital inputs [4], [5], [9]–[14]. These circuits work properly only as long as all transistors are kept in the saturation region, which means that they need a minimum voltage of $V_{D\,\mathrm{sat}}$, defined in (1), across their drain-source terminals (even though the following discussion is based on the nMOS transistors, it also applies to the duals of these circuits with pMOS transistors)

$$V_{D\,\mathrm{sat}} = \sqrt{\frac{2I_D L}{K_P W}} \tag{1}$$

where I_D is the drain current, K_P is the intrinsic transconductance, and W and L are the MOS transistor width and length, respectively. Obviously, $V_{D\,\mathrm{sat}}$ increases with higher stimulation currents, even though it can be reduced by increasing the width of the MOS transistor at the expense of more area consumption. If a simple current mirror is used for stimulation, as shown in Fig. 1(a), a maximum voltage of $V_{\mathrm{CC}} - V_{D\,\mathrm{sat}}$ could be built up across the tissue, which is referred to as the voltage compliance of a simple current mirror. Meanwhile, the circuit dissipates $V_{D\,\mathrm{sat}}(I_D + V_{D\,\mathrm{sat}}/r_o)$ of power in transistor M_1, where $r_o = 1/\lambda I_D$ is the output resistance of M_1 as well as the entire current source, and λ is the channel length modulation factor of M_1. The output resistance of a simple current mirror, r_o, is not high enough for biomedical microstimulation applications, especially when it decreases at high currents, and causes the stimulus current to vary considerably with output voltage variations.

Fully cascode (FC) and wide swing cascode (WSC) current mirrors, shown in Fig. 1(b) and (c), respectively, are used in many designs, including [9]–[14], to increase the current source output resistance by a large factor. These current mirrors increase the output resistance by a factor of $g_m r_o$, where $g_m = (2I_D K_P W/L)^{0.5}$ is the cascode transistor (M_3) transconductance. Increased output resistance, however, comes at the expense of reduced voltage compliance to $V_{\mathrm{CC}} - V_{D\,\mathrm{sat}} - V_{\mathrm{THn}}$ and $V_{\mathrm{CC}} - 2V_{D\,\mathrm{sat}}$ (neglecting the body effect) in FC and WSC current sources, respectively [18]. It also increases the power dissipation in saturated transistors to $I_D(V_{D\,\mathrm{sat}} + V_{\mathrm{THn}})$ and $2I_D V_{D\,\mathrm{sat}}$, where V_{THn} is the nMOS threshold voltage. Unfortunately, the body effect only worsens the above situation by increasing V_{THn}.

B. Proposed Stimulation Circuit

The proposed stimulation circuit is based on the voltage-to-current conversion topology of Fig. 2, [17]. In this circuit, the voltage across R is kept constant at V_{in} by a negative feedback,

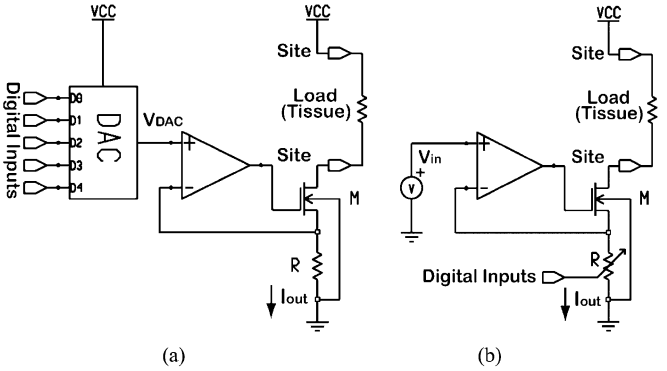

Fig. 2. Stimulation with voltage to current conversion circuit. (a) Controlling the stimulus current by input voltage $(\mathrm{V_{in}})$. (b) Controlling the stimulus current by switching the resistor (R).

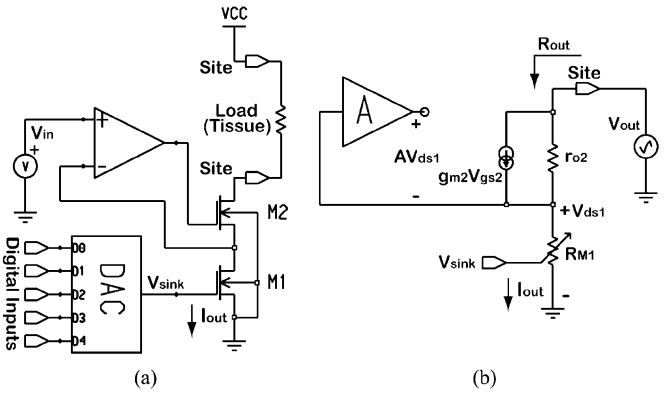

Fig. 3. (a) Simplified topology of the VCR current source, which utilizes M1 in deep triode region as a voltage controlled resistor. (b) Small signal equivalent of the circuit shown in (a).

and the output current, $I_{\mathrm{out}} = V_{\mathrm{in}}/R$, can be controlled by either V_{in} or R as shown in Fig. 2(a) and (b), respectively. The voltage compliance of this voltage-controlled current source can be as high as $V_{\mathrm{CC}} - V_{\mathrm{in}}$, if the OpAmp gain and the size of transistor M are large enough [18]. Controlling I_{out} by V_{in}, as suggested in [19], is not desirable in this application since it changes the current source voltage compliance as well. Nevertheless, choosing a small constant value for V_{in}, and controlling I_{out} by changing R, provides a large constant voltage compliance for a wide range of output currents. The best available choice for implementing the variable resistor R in this CMOS-IC design is an nMOS transistor, biased in deep triode region. The nMOS dynamic resistance changes almost linearly with its V_{GS} voltage in the triode (linear) region, and consequently controls the output current. This results in the basic topology of our proposed circuit in Fig. 3(a). As long as M_1 is kept in the triode region, the output current in this circuit will be defined by (2), with a well known linear relationship with V_{GS1}, which is supplied by a voltage-mode DAC, and called V_{sink} in Fig. 3(a)

$$I_{\mathrm{out}} = K_P \frac{W_1}{L_1}\left(V_{\mathrm{sink}} - V_{\mathrm{THn}} - \frac{1}{2}V_{\mathrm{in}}\right)V_{\mathrm{in}}. \tag{2}$$

M_1 operates in the triode region as long as $V_{\mathrm{DS1}} = V_{\mathrm{in}} < (V_{\mathrm{sink}} - V_{\mathrm{THn}})$. Therefore, a smaller V_{in}, provides a larger current source voltage compliance $(V_{\mathrm{CC}} - V_{\mathrm{in}})$ and a wider range of V_{sink} voltages, where M_1 stays in the triode region, both of which are desirable. The only cost is the circuit area, which should be increased by increasing W_1/L_1 according to (2) in order to achieve the desired stimulus current levels.

Nevertheless, it will be shown that the required area is still about two orders of magnitude less than what would be needed to achieve a comparable performance using the conventional current sources. What is done here in solid-state physics terms, is that instead of pinching off the saturated MOS channel, and passing the stimulus current through a very thin layer on the MOS channel surface in conventional current sources, M_1 of the VCR current source is biased in the triode region to provide a deep inverted channel as a result of applying a large gate voltage (V_{sink}). V_{sink} then controls the inverted channel depth, and consequently the stimulus current. Therefore, the density of stimulus current per unit channel width (μA/μm) in the VCR current source is much higher than any conventional current source with saturated transistors.

A comparison between the voltage compliance at full-scale current (250 μA) of three current source designs, the FC, WSC, and VCR (Figs. 1(b), (c) and 3), is carried out using the SPICE parameters from the AMI 1.5-μm standard CMOS process [20]. It is shown in Section III, (Fig. 9) that with a 5-V supply, the VCR current source can achieve a voltage compliance of 4.85 V at full-scale current by choosing $V_{\mathrm{in}} = 80$ mV and $V_{\mathrm{sink}} = 4.5$ V. The FC design cannot achieve more than $V_{\mathrm{CC}} - V_{\mathrm{THn}} = 4.39$ V of compliance voltage no matter how large its transistors are made. For the WSC design, $V_{D\,\mathrm{sat}}$ in (1) should be limited to 75 mV to achieve $V_{\mathrm{CC}} - 2V_{D\,\mathrm{sat}} = 4.85$ V compliance. Equating the full-scale currents of the VCR and WSC current sources

$$I_{\max} = K_P \left(\frac{W}{L}\right)_{\mathrm{VCR}} \left(V_{\mathrm{GS1}} - V_{\mathrm{THn}} - \frac{V_{\mathrm{in}}}{2}\right) V_{\mathrm{in}} = \frac{K_P}{2} \left(\frac{W}{L}\right)_{\mathrm{WSC}} V_{D\,\mathrm{sat}}^2 \tag{3}$$

shows that each of the saturated WSC transistors [M_1–M_4 in Fig. 1(c)] should be 110 times larger than M_1 of the VCR current source in the triode region. This comparison shows that the VCR current source can significantly save silicon active area especially when the stimulus current levels are high.

The output impedance of the VCR current source can be derived from its small signal equivalent circuit in Fig. 3(b)

$$R_{\mathrm{out}} = A g_{m2} r_{o2} R_{M1} \tag{4}$$

where A is the operational transconductance amplifier (OTA) gain, R_{M1} is the VCR implemented by M_1, and g_{m2} and r_{o2} are the transconductance and output resistance of M_2, respectively. Since V_{in} is small (80 mV), its second order term can be neglected in (2), and R_{M1} is given by

$$R_{M1} = \frac{L_1}{K_P W_1 (V_{\mathrm{GS1}} - V_{\mathrm{THn}})}. \tag{5}$$

The output impedance of an FC current source is $g_{m2} r_{o2} r_{o1}$ [18], which is usually higher than the WSC output impedance. Therefore, if the VCR current source OTA is designed with enough gain such that $AR_{M1} = r_{o1}$ then according to (4) both sources will show equal output impedance. In our design, R_{M1} has a minimum value of 320 Ω (80 mV/250 μA) and r_{o1} is about 175 kΩ. Therefore, A needs to be above 55 dB for the VCR current source output impedance to exceed that of the FC current source. The simulated output current versus stimulating site voltage curves of the conventional current sources, shown in Fig. 1, and the VCR current source is shown in Fig. 4. In this comparison which is also summarized in Table I, all current sources were designed to roughly occupy the same area on chip

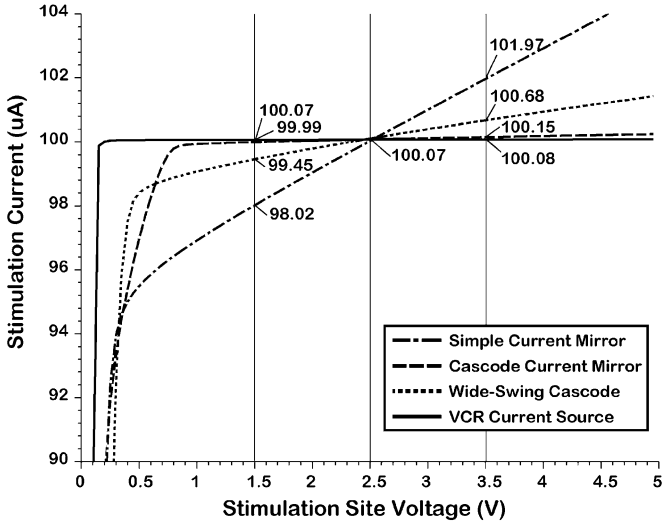

Fig. 4. A comparison between the output characteristics of the conventional current sources shown in Fig. 1 and the VCR current source. Design criteria: 1—Occupy roughly the same area on chip ($\sim$0.1 mm2) 2—Sink 100 μA when the site voltage is 2.5 V ($\mathrm{V_{CC}} = 5$ V).

TABLE I
COMPARISON BETWEEN DIFFERENT CURRENT SOURCES THAT OCCUPY THE SAME AREA

Current source*	Output impedance (MΩ)	Voltage compliance (V)
Simple current mirror	0.5	4.3
Fully cascode	12.7	4.1
Wide swing cascode	1.63	4.5
VCR	200	4.85

* $\mathrm{I_{Sink}}$ = 100 µA when stimulation site voltage is 2.5 V, Area ≈ 0.125 mm^2, V_{CC} = 5 V.

($\sim$0.1 mm^2), and sink 100 μA when the stimulating site voltage is 2.5 V. It is obvious from Fig. 4 curves that the VCR current source has the closest output characteristics to an ideal current source.

III. CIRCUIT IMPLEMENTATION

The basic theory and topology of the VCR current source, described in Section II, were simple. However, several design considerations need to be addressed for this circuit to be implemented in a way that complies with the high level of medical-grade standards. In this section, the circuit implementation is reviewed in more detail by addressing these requirements.

A. Reference Generator

The reference generator circuit (Fig. 5) is based on a thermal voltage self-biasing topology that provides a high degree of supply voltage independence [18], which is important in both inductively coupled and battery-powered implants. In the former, relative movements between the external and implanted coils significantly change the received power, and in the latter, the battery voltage decreases over time from fully charged to exhausted levels. This block generates a reference current $(\mathrm{I_{ref}})$ for a current steering DAC, biasing voltages $(\mathrm{V_{bn1}}, \mathrm{V_{bn2}}, \mathrm{V_{bp1}}, \mathrm{V_{bp2}})$ for cascode current mirrors used in OTAs (Fig. 7), a band-gap reference voltage $(\mathrm{V_{gap}})$ for calibration, and two voltages close to each supply rail, $\mathrm{V_{low}} = \mathrm{V_{in}} = 80$ mV and $\mathrm{V_{high}} = \mathrm{V_{CC}} - \mathrm{V_{in}} = 4.92$ V, for the nMOS VCR current sink and a similar pMOS VCR current source, respectively. The reference generator layout is equipped with several laser-cutting links for fine-tuning its reference voltages and currents.

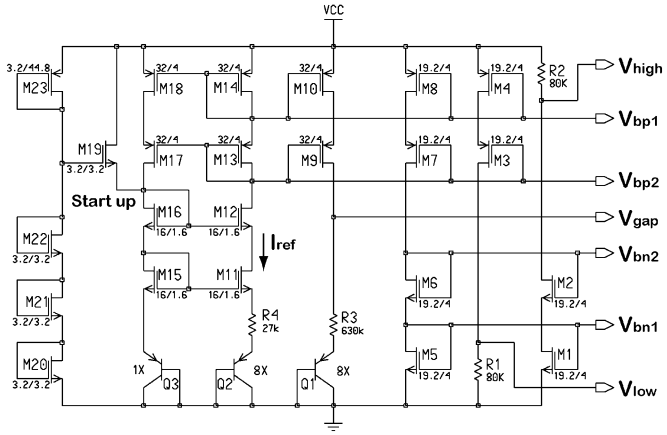

Fig. 5. Reference generator circuit based on thermal voltage self-biasing topology [18].

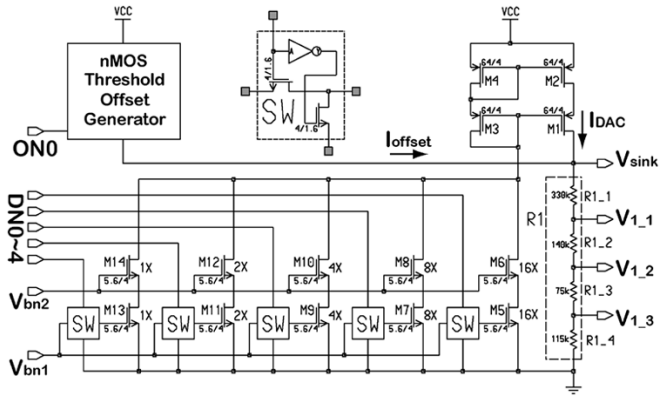

Fig. 6. A 5-bit voltage-mode current steering DAC, used to generate nMOS gate voltages required to control the VCR current source.

B. Digital-to-Analog Converter

Fig. 6 shows the 5-bit current steering DAC, which provides digital control over $V_{\rm sink}$ in 32 steps ($\sim$115 mV each) from $V_{\rm THn}$ up to about 4.3 V, where $\rm M_1$–$\rm M_4$ go out of saturation. A scaled version of $I_{\rm ref}$ is multiplied by powers of 2, through 5.6 μm/4 μm nMOS transistors repeated in parallel, in order to generate a current, $I_{\rm DAC}$, proportional to the digital input ($\rm DN_0$–$\rm DN_4$). This current then adds to an offset current ($I_{\rm offset}$), and passes through R_1 resistor string to generate $V_{\rm sink}$ and its fractions, $V_{\rm 1\text{-}1} - V_{\rm 1\text{-}3}$, which are the gate voltages of $\rm M_{1\text{-}1} - M_{1\text{-}3}$ in Fig. 8, which are used to linearize the VCR current source

$$V_{\rm sink} = R_1(I_{\rm DAC} + I_{\rm offset}). \quad (6)$$

In a multichannel microstimulating system [21], a single DAC (including R_1) can control several VCR current sources, unless simultaneous stimulus currents with different amplitudes are needed.

C. Operational Transconductance Amplifier

The OTA feedback loop serves two purposes in a VCR current source. First, it keeps the $\rm M_1$ drain voltage at $V_{\rm in} = V_{\rm low}$, and second, it significantly increases the current source output resistance according to (4). A pMOS-input folded-cascode OTA was used, as shown in Fig. 7, to provide a large gain at small common mode input voltages. Simulation results show that the OTA provides more than 74-dB gain at $V_{\rm in} = 80$ mV common mode input, which is well above the minimum 55-dB gain required by (4).

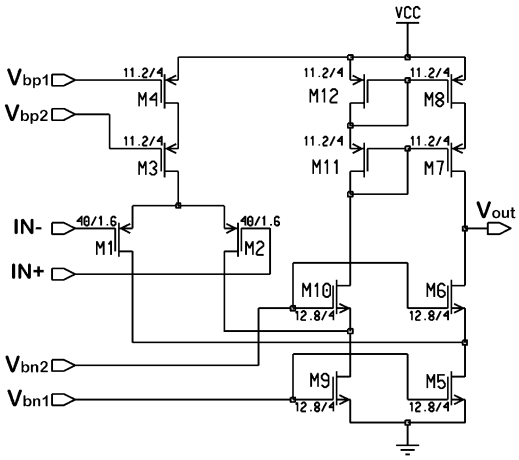

Fig. 7. pMOS-input folded-cascode OTA with 74-dB gain at 80 mV common-mode input.

D. Current Source Linearity

Current source linearity in biomedical microstimulating applications is not as critical as it is in DAC and ADC circuits used in audio or communication applications, where it directly affects the distortion level. Firstly, because biological systems are highly nonlinear, and their response to electrical stimulation varies with several other parameters, including the signal amplitude. Secondly, any kind of nonlinearity in the stimulator, provided that it is persistent, can be corrected for by the system software, which might use a look-up table to generate stimulation pulses at a desired level. Yet, having a linear relationship between the DAC digital input and the stimulus current in the VCR current source can highly facilitate its usage in a larger system as well as improve the charge balancing capability of the microstimulator [12], [21].

If the secondary effects could be neglected, the relationship between $\rm M_1$ drain current ($I_{\rm out}$) and its gate voltage ($V_{\rm sink}$) in the triode region would already be linear as stated in (2). However, three types of nonlinearity become evident as $V_{\rm sink}$ is swept from zero to $V_{\rm CC}$.

1) For $0 < V_{\rm sink} < V_{\rm THn}$, $\rm M_1$ is off and $I_{\rm out} = 0$. Adding an offset current ($I_{\rm offset}$) to $I_{\rm DAC}$ according to (6), which generates an offset voltage equal to $V_{\rm THn}$ across the resistor R_1 in Fig. 6, always sets the zero digital input value of the DAC output voltage to $V_{\rm sink}(0) = V_{\rm THn}$.
2) For $V_{\rm THn} < V_{\rm sink} < V_{\rm in} + V_{\rm THn}$, transistor $\rm M_1$ goes into saturation and $I_{\rm out} = K_P(W_1/L_1)(V_{\rm GS1} - V_{\rm THn})^2/2$. This nonlinearity is not important since $V_{\rm in}$ (80 mV) is even smaller than a single DAC voltage step ($\sim$115 mV), and it is easily stepped over by the DAC.
3) For large $V_{\rm sink}$ values, $I_{\rm out}$ is less than what is predicted by (2). Especially when $V_{\rm sink}$ is close to $V_{\rm CC}$, simulations with BSIM3v3 model show that $I_{\rm out}$ is almost half of (2). The main reason for this nonlinearity is the carrier mobility degradation due to the high vertical field that is set up by large gate-body potential in $\rm M_1$. This effect is depicted in SPICE level-3 as the effective mobility

$$\mu_{\rm eff} = \frac{\mu_o}{1 + \theta(V_{\rm sink} - V_{\rm THn})} \approx \mu_o(1 - \theta(V_{\rm sink} - V_{\rm THn})) \quad (7)$$

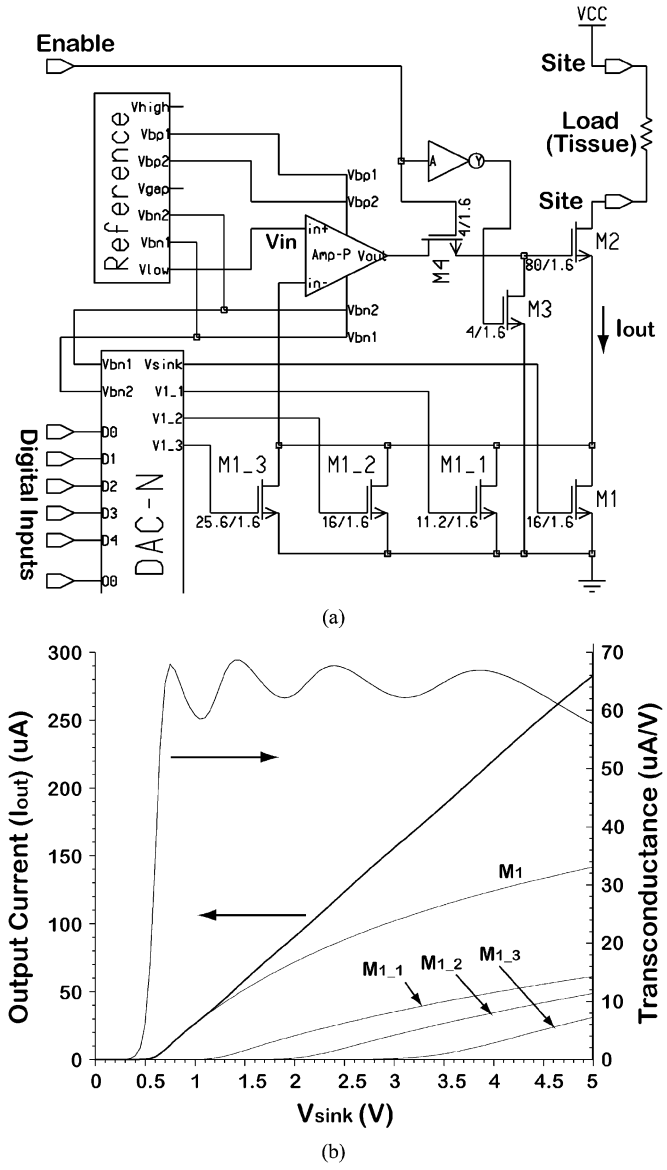

Fig. 8. (a) Detailed schematic diagram of the VCR current source. (b) Linearized output of the VCR current source versus $\mathrm{V_{sink}}$ input voltage. $\mathrm{I_{out}}$ is the sum of four parallel nMOS drain currents, denoted as M1–M1-3. The 2nd vertical axis shows the slope of Iout, which is a measure of the VCR current source linearity.

where μ_0 is the low-field bulk mobility, and θ is the mobility degradation factor [18].

There has been much effort to linearize the MOS current in terms of V_{DS} in the triode region to use MOS transistors as large resistors in IC filters [19], [22], [23]. In the VCR current source, however, V_{DS1} is kept constant at V_{in}, and the goal is to linearize I_{out} versus V_{sink}. Substituting (7) in (2) ($K_P = \mu_{\mathrm{eff}} C_{\mathrm{ox}}$, where C_{ox} is the gate oxide capacitance) shows the reduction of I_{out} from its linear trace at high V_{sink}. On the other hand, MOS drain current goes above the linear trace versus V_{GS} when it is biased in saturation. This suggests that if we combine the drain current of $\mathrm{M_1}$ in deep triode region with another transistor (denoted by $\mathrm{M_{1\text{-}1}}$) in saturation region, even though the individual transistor currents are nonlinear, their sum can be tailored to be linear versus V_{sink}. Analytically, we consider the first two terms of the Taylor series expansion of (7) in terms of $V_{\mathrm{sink}} - V_{\mathrm{THn}}$, and substitute them in (2) to find $\mathrm{M_1}$ drain current. We also apply a fraction (k) of V_{sink} to $\mathrm{M_{1\text{-}1}}$ gate terminal to bias it in the saturation region, and then add the drain currents

$$I_{\mathrm{out}} = K_{P0}\frac{W_1}{L_1}\left((V_{\mathrm{sink}} - V_{\mathrm{THn}})V_{\mathrm{in}} - \frac{1}{2}V_{\mathrm{in}}^2\right) \times (1 - \theta(V_{\mathrm{sink}} - V_{\mathrm{THn}})) + K_{P0}\frac{W_{1\text{-}1}}{L_{1\text{-}1}}(kV_{\mathrm{sink}} - V_{\mathrm{THn}})^2 \quad (8)$$

where $K_{P0} = \mu_0 C_{\mathrm{ox}}$. To achieve a linear equation in terms of V_{sink}, the negative coefficient of V_{sink}^2 in the first term of (8) should cancel out with the positive coefficient of V_{sink}^2 in the second term. Therefore

$$k = \sqrt{\frac{W_1 L_{1\text{-}1}}{W_{1\text{-}1} L_1}\theta V_{\mathrm{in}}}. \quad (9)$$

Although (9) provides an analytical guideline to find a proper size $(W_{1\text{-}1}/L_{1\text{-}1})$ and gate voltage ratio (kV_{sink}) for the parallel linearizing transistor $(\mathrm{M_{1\text{-}1}})$, it has several limitations. First, the Taylor expansion that was used in (7) only applies when V_{sink} is close to V_{THn}, which is not the case in the entire V_{sink} range. Second, $\mathrm{M_{1\text{-}1}}$ stays in saturation only in a certain segment of the V_{sink} range due to its small $V_{\mathrm{DS1-1}} = V_{\mathrm{in}}$. Below this segment, $\mathrm{M_{1\text{-}1}}$ is off, and above it, $\mathrm{M_{1\text{-}1}}$ goes into the triode region, and shows a nonlinear relationship with kV_{sink}, similar to $\mathrm{M_1}$. Third, there are several other secondary effects that affect I_{out} in the entire V_{sink} range that have been ignored in the above simplified analysis.

A more practical approach to overcome these limitations is to use (9) to find an approximate value for k and $W_{1\text{-}1}/L_{1\text{-}1}$. Then use simulation tools to fine-tune a linear relationship between I_{out} and V_{sink}. When $\mathrm{M_{1\text{-}1}}$ goes out of saturation, the above procedure can be used iteratively to size another parallel transistor, $\mathrm{M_{1-2}}$, with a smaller fraction of V_{sink} on its gate to linearize an upper segment of the I_{out}-V_{sink} curve. The result of this approach is the VCR current source of Fig. 8(a), whose I_{out}-V_{sink} curve in Fig. 8(b) is linearized with 3 auxiliary parallel transistors ($\mathrm{M_{1\text{-}1}}$–$\mathrm{M_{1\text{-}3}}$). Fig. 8(b) also shows the contribution of each individual parallel MOS transistor in I_{out}, which is the sum of all four drain currents. It can be seen that the original transistor, $\mathrm{M_1}$, is always 'on' and mostly in deep triode region for $V_{\mathrm{sink}} > V_{\mathrm{THn}}$. The other auxiliary transistors, which receive increasingly smaller fractions of V_{sink} from the DAC resistive voltage divider string, turn on at a certain V_{sink} level, stay in saturation in a certain segment of V_{sink} range defined by

$$V_{\mathrm{THn}} + V_{\mathrm{in}} > \left(\sum_{j=i+1}^{4} R_{1-j}/R_1\right) V_{\mathrm{sink}} > V_{\mathrm{THn}} \Rightarrow M_{1-i}(\mathrm{sat}) \quad \text{where } R_1 = \textstyle\sum_{j=1}^{4} R_{1-j} \quad (10)$$

while linearizing the sum of previously 'on' parallel MOS transistors, and finally go into triode region for the rest of V_{sink}. The right vertical axis of Fig. 8(b) shows the slope of I_{out}-V_{sink} curve $(dI_{\mathrm{out}}/dV_{\mathrm{sink}})$, which is the transconductance of the VCR current source (average 64.7 μSiemens). The transconductance curve is a measure of the VCR current source linearity, and the effect of each parallel transistor is evident from one of the peaks in this curve. Increasing the number of parallel auxiliary transistors reduces the transconductance ripple at the expense of a larger circuit area.

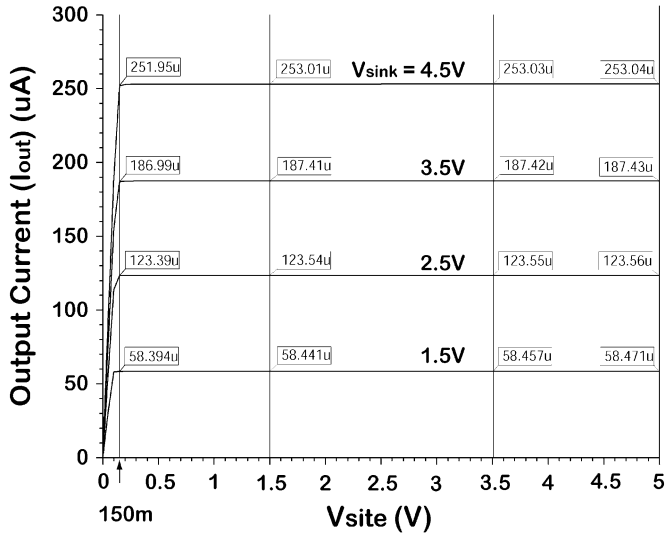

Fig. 9. Output current versus stimulating site voltage for different $\mathrm{V_{sink}}$ input voltages. These curves show the high voltage compliance (>4.85 V) and output impedance ($1.5\ \mathrm{V} < \mathrm{V_{site}} < 3.5$ V, $1/\mathrm{slope} \geq 100\ \mathrm{M\Omega}$) of the VCR current source.

E. Voltage Compliance and Output Impedance

To show the large voltage compliance and high output impedance of the VCR current source, V_{sink} was changed from 1.5 V to 4.5 V in 1-V steps, and the stimulating site voltage (V_{site}) was swept from ground to V_{CC}, while monitoring I_{out}. According to (4), R_{out} is minimum at full-scale current because R_{M1} (5) and $r_{o2} = 1/\lambda I_{\mathrm{out}}$ are both minimum, and this is usually the situation when the maximum voltage compliance of a microstimulator is utilized. It can be seen in Fig. 9 that I_{out} is kept constant within 1% of its nominal value in a 4.85-V span of V_{site} from V_{CC} down to 150 mV, and R_{out}, which is the reciprocal of I_{out} slope $(dV_{\mathrm{site}}/dI_{\mathrm{out}})$ is mostly above 100 MΩ in this voltage span.

F. Process Variations

Threshold voltage (V_{THn}) and sheet resistance $(R_{\square})$ are the two process dependent parameters that are most effective on the VCR output current according to (2) and (6). Each of these parameters can change up to 35% from one fabrication run to another [20], [24]. V_{THn} vertically shifts the entire I_{out} versus V_{sink} curve as an offset, while $R_{\square}$ changes the DAC gain and reference output voltages ($V_{\mathrm{low}}, V_{\mathrm{high}}$, and V_{gap}), and therefore, affects the VCR current source transconductance. The following provisions are made in the circuit design to compensate for process variations:

1) To compensate for V_{THn} variations, a threshold reference self-biasing circuit [18], shown in Fig. 10(a), generates an offset current

$$I_{\mathrm{offset}} = V_{\mathrm{GS6}}/nR_{\mathrm{of}} \tag{11}$$

where n is the offset current scaling ratio. I_{offset} adds to I_{DAC} in Fig. 6, and passes through R_1 resistor string. In Fig. 10(a), if $\mathrm{M_6}$ is large enough, then $V_{\mathrm{GS6}} \approx V_{\mathrm{THn}}$, and if n is chosen equal to $R_1/R_{\mathrm{of}} \approx 2$, then according to (6), I_{offset} generates an offset voltage equal to V_{THn} across R_1, which compensates V_{THn} variations in I_{out}, and also eliminates the first type of nonlinearity that was described in Section III-D. To provide more flexibility over the offset current adjustments, a digital control bit $(\mathrm{ON_0})$ is dedicated to n, which can be used to add an offset to the stimulus current. Fig. 10(b) compares variations in $\mathrm{M_1}$ and $\mathrm{M_2}$ drain currents in Fig. 8(a) with and without I_{offset}, when V_{THn} is changed from 0.4 to 0.7 V [20]. It can be seen that I_{offset} increases linearly with V_{THn}, and reduces I_{D1} and $I_{D2} = I_{\mathrm{out}}$ variations from 29.3% and 41.5% to 0.75% and 12.5%, respectively.

2) In order to compensate for sheet resistance $(R_{\square})$ variations, all resistors are laid out in the same type of resistive layer (polysilicon). I_{ref} in Fig. 5 is inversely proportional to $R_{\square}$. However, all other reference and DAC output voltages are directly proportional to $R_?$ as well as I_{ref}. Therefore, even though I_{ref} changes with $R_{\square}$ variations, $R_{\square}$ cancels out in all voltages that control the performance of the VCR current source. I_{ref} variations also affect the OTA biasing currents as well as its gain (A). However, the VCR output impedance is so high that variations in A have little effect on the overall performance of the system.

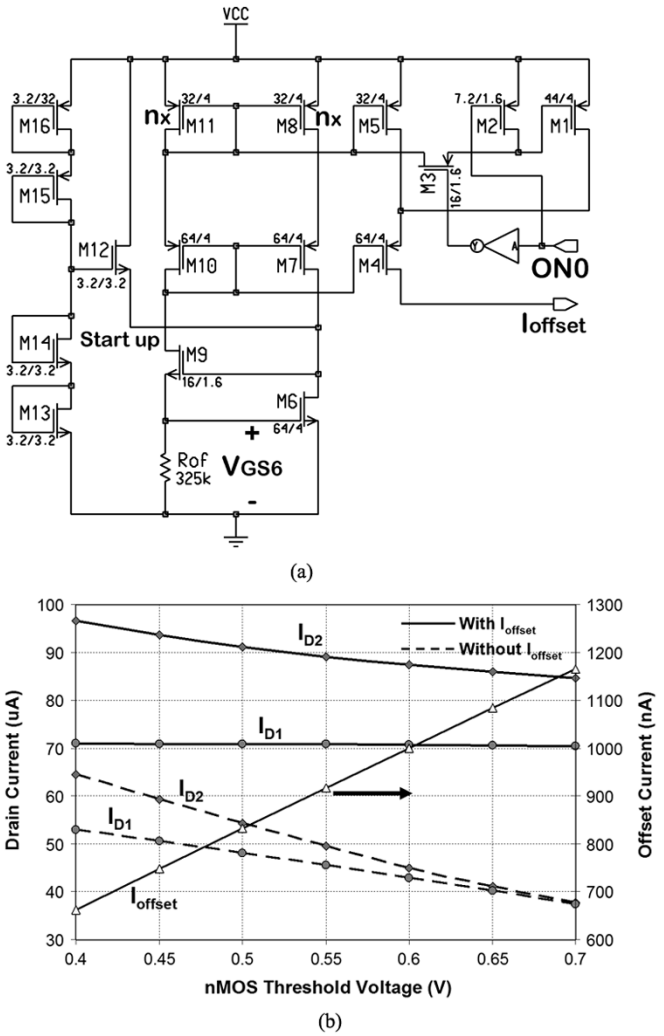

Fig. 10. (a) Offset current ($\mathrm{I_{offset}}$) generator circuit based on threshold voltage self-biasing topology [18]. (b) A comparison between M1 and M2 drain current variations in Fig. 8(a) versus VTHn with and without the offset generator block.

G. Matching and Charge Balancing

Matching among stimulating channels and charge balancing are important issues regarding safety and durability of implantable microstimulators, especially in multichannel systems.

For monopolar stimulation in a hardwired microstimulator, which means sourcing (sinking) current from (to) a stimulating site to (from) a large, distant grounded electrode, charge balancing requires using both pMOS VCR current source and nMOS VCR current sink circuits, connected to positive and negative supply rails, respectively [9]. In wireless microstimulators, however, to reduce power consumption, it is possible to do bipolar stimulation between two stimulating sites by switching a single supply, as long as the implant is electrically floated in the tissue [4], [5], [10], [11]. In a prototype chip, designed as a precursor to a wireless microstimulating system [21], four stimulating sites are implemented that each one is driven by an individual site driver circuit, shown in Fig. 11(a). A_i and $B_i(i = 0\text{-}3)$ are two digital control bits, dedicated to each site driver, which can connect each site to $V_{\rm CC}$, an nMOS VCR current sink, a common analog line (CAL), or leave it at high impedance (high-Z) as shown in Fig. 11(b), and summarized in Table II, [15], [16]. Initially all the sites are in the high-Z state, and all the switches in Fig. 11(a) are open except $\rm S_1$, which keeps $\rm M_2$ off. No current can leak into or out of the sites that are in the high-Z state, since they are completely disconnected from the rest of the circuits.

During the cathodic phase of a biphasic bipolar stimulation (between site-0 and site-3 for example), whose current waveform is shown in Fig. 11(c), $\rm S_4$ connects site-0 to $V_{\rm CC}$, while $\rm S_2$ activates the VCR current sink associated to site-3. The high output impedance of the VCR current sink adjusts site-3 voltage somewhere between $V_{\rm CC}$ and 0.15 V such that irrespective of site-0, surrounding tissue, and site-3 impedances, the desired amount of stimulus current $(I_{\rm out3})$ passes through the tissue from site-0 to site-3. At the end of the cathodic phase (T_c), both sites go back to the high-Z state for an interphase delay (T_i) and, therefore, no current passes through the tissue. For the anodic phase (T_a), the sites states are swapped by connecting site-3 to $V_{\rm CC}$ and activating site-0 VCR current sink. Therefore, the stimulus current $(I_{\rm out0})$ passes in the opposite direction from site-3 to site-0.

For charge balancing, one should ensure that the total amount of charge that is injected into the tissue is equal to zero. Quantitatively, according to Fig. 11(c)

$$Q_c = I_{\rm out3}T_c = I_{\rm out0}T_a = Q_a \tag{12}$$

where Q_c is the charge injected in the cathodic phase and Q_a is the charge injected during the anodic phase. Assuming that the digital timing circuitry (not included in the prototype chip) is accurate $(T_c = T_a)$, charge balancing narrows down to the matching between the two VCR current sinks, which receive the same digital input command. Several designers have got around this problem by multiplexing a single current source between several stimulating sites at the expense of losing the flexibility of having multiple simultaneous active channels [4], [10], [11]. The small size of the VCR circuit allows each stimulating channel to have an individual current sink. However, this is not enough for multiple simultaneous active pairs, since the current through the sourcing sites, which are directly connected to $V_{\rm CC}$, is not controlled, and low impedance sites might be forced to source most of the total current, and exceed the safe charge injection limits [25]. For multiple simultaneous active sites, each channel should be equipped with both current sink and current source circuits, such that the current passing through each site, whether sourcing or sinking, would be controlled [21]. The current spread among the active pairs would be still defined by the volume conductor (tissue), especially if they are in close proximity (multipolar stimulation).

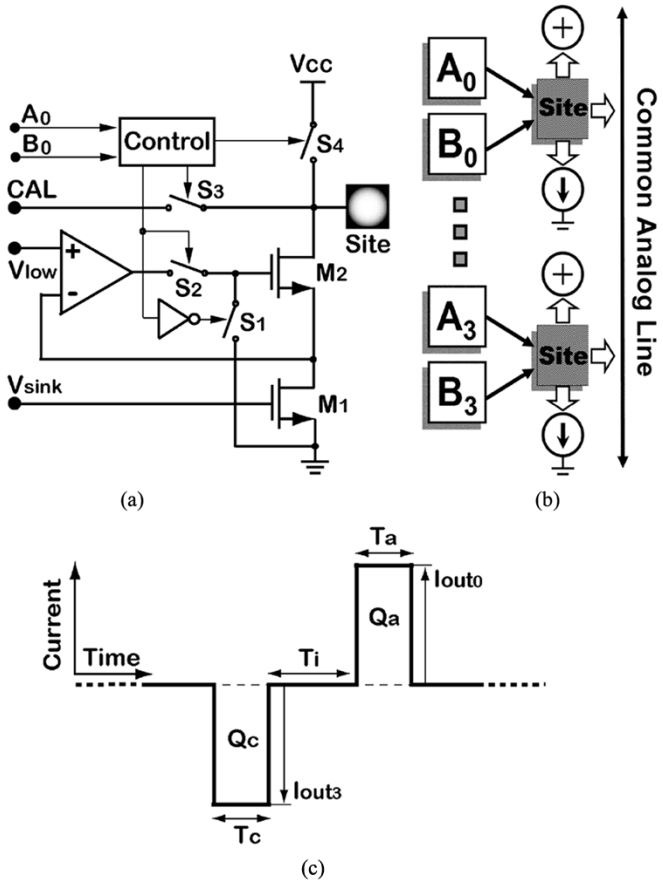

Fig. 11. (a) A simplified site driver schematic. (b) Each stimulating site can be connected to VCC, a VCR current sink, CAL, or left at high-Z (see Table II), controlled by 2 bits (Ai, Bi). (c) Current waveform in a biphasic bipolar stimulation between two sites.

TABLE II
STIMULATING SITE STATUS AND FUNCTIONS

State	A	B	Closed Switches in Fig. 11a	Function
0	0	0	S_1	High impedance
1	0	1	S_1 and S_4	V_{CC}
2	1	0	S_2	nMOS-VCR current sink
3	1	1	S_1 and S_3	Common analog line (CAL)

In the prototype system, all VCR current sinks are controlled with the same DAC and reference generator blocks. Therefore, $V_{\rm sink}, V_{\text{1-1}} - V_{\text{1-3}}$, and $V_{\rm low}$ are the same for the active pair. The only types of mismatch that can occur are due to the difference between OTA input offset voltages, process related geometrical mismatches, and parameter variations across the chip. In order to minimize these mismatches, site driver blocks were laid out side by side, as shown in Fig. 12. Moreover, to exhaust all the residual charges stored in the tissue due to these small mismatches, after a certain number of stimulations, all sites can be shorted together through the CAL by putting all of them in state 3 (see Table II), [9].

IV. EXPERIMENTAL RESULTS

The prototype 2.2 mm $\times$ 2.2 mm chip was fabricated in the AMI 1.5-μm, 2-metal, 2-poly, n-well, standard CMOS process.

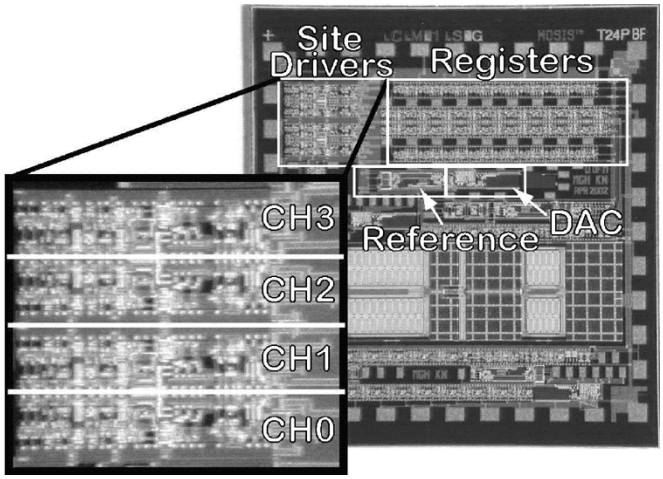

Fig. 12. A prototype chip with four VCR stimulating channels, fabricated in the AMI 1.5-μm standard CMOS process.

TABLE III
SIMULATED AND MEASURED SPECIFICATIONS OF THE VCR STIMULATING CIRCUIT

Parameter	Simulation	Measurement
V_{low}	0.39 V	0.58 V
V_{gap}	1.32 V	1.39 V
Reference current (I_{ref})	11.22 µA	12.4 µA
Voltage compliance	4.4 V	4.25 V
Output impedance (R_{out})	18.8 MΩ	>10 MΩ*
Max stimulation current (I_{max})	155 µA	210 µA
Current consumption	43 µA	**

* The exact value was out of the dynamic range of our measurement equipment.
** We were unable to isolate the current consumption of the stimulator block from the rest of the chip.

Fig. 12 shows a die photograph of the chip and its floor plan, which also contains other individual blocks of the wireless microstimulating system that are not covered in this paper [21]. Fig. 12 inset shows a magnified view of the four site drivers, which schematic is shown in Fig. 11. Each site driver block, is capable of sinking up to 210 μA, and occupies 0.05 mm^2 of the chip area. Table III summarizes some of the simulated (design targets) versus measured specifications. It should be noted that $V_{\rm low}$ in this chip is much larger than the desired value (80 mV) in our improved design that was described in Section III. However, the experimental results still demonstrate the advantages and the idea behind the VCR current source.

Fig. 13 shows the measured 5-bit DAC output voltage ($V_{\rm sink}$), and VCR output currents ($I_{\rm out}$) for the four individual site drivers, passing through 10 kΩ resistors that represent tissue between two stimulating sites, versus DAC digital input. Even though only one auxiliary transistor ($\rm M_{1\text{-}1}$) is used in parallel to $\rm M_1$, the output current is fairly linear except for $V_{\rm sink} < V_{\rm low} + V_{\rm THn} \approx 1.2$ V, where $\rm M_1$ is in saturation. The width of this region, however, is significantly reduced in the improved design by decreasing $V_{\rm low}$ from 0.58 to 80 mV, as discussed in Section III-D and simulated in Fig. 8(b). Fig. 13 curves also show a very good matching with less than 7% difference among different VCR current sinks through the entire $V_{\rm sink}$ range. To measure the voltage compliance and output impedance of the VCR current sinks, at several constant digital inputs, the site voltage was swept from 0 to 5 V using an HP4155A semiconductor parameter analyzer, while measuring $I_{\rm out}$ similar to Section III-E. The resulting curves in Fig. 14 show that in the worst case, the full-scale $I_{\rm out}$ is kept constant

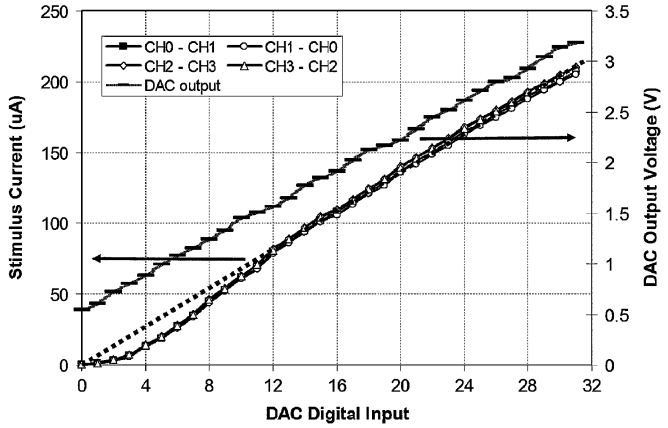

Fig. 13. Measured VCR stimulus current for four individual channels, and 5-bit DAC output voltage (Vsink) versus DAC digital input.

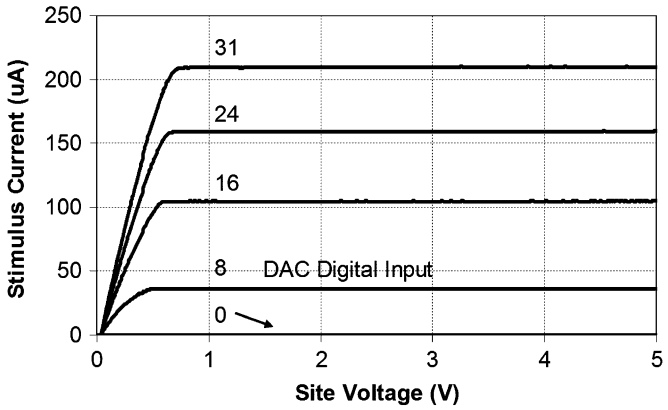

Fig. 14. Measured VCR output current ($\rm I_{out}$) versus stimulating site voltage, swept from ground to VCC at different DAC digital inputs.

within 1% of its nominal value in a 4.25-V span of $V_{\rm site}$ from $V_{\rm CC}$ down to 0.75 V, and $R_{\rm out}$ is above the accuracy of the measurment equipment (>10 M Ω) in this range.

V. CONCLUSION

We have made key improvements in the design of CMOS current sources that are suitable for implantable microstimulators by significantly increasing the output impedance and voltage compliance of these circuits, while decreasing their chip area consumption. The new current source utilizes MOS transistors in deep triode region as linearized voltage controlled resistors. The stimulus current is controlled by the MOS gate voltage, which is digitally programmable by a voltage-mode DAC. We were able to show large voltage compliance of up to 97% of the supply voltage, and high output impedance in the 100 MΩ range to keep the stimulus current constant within 1% of the desired value, irrespective of the highly variable site and tissue impedances. This new approach is particularly useful at low supply voltages, and saves significant chip area compared to the conventional methods, especially when the stimulation current level is high in the milliampere range. A 4-channel prototype chip was fabricated in the AMI 1.5-μm standard CMOS process, and even though the design parameters were not optimized, it could show the advantages of the VCR current source in experimental results. With a 5-V supply, each site driver maintained up to 210 μA with less than 1% variation in a 4.25-V site voltage span, and occupied 0.05 mm2 of the chip area.

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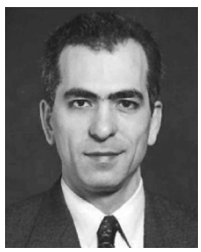
Maysam Ghovanloo (S'00–M'04) was born in 1973. He received the B.S. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 1994, and the M.S. (Hons.) degree in biomedical engineering from the Amirkabir University of Technology, Tehran, in 1997. He also received the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 2003 and 2004, respectively. His undergraduate research was focused on developing an 8-kW power supply for Nd:YAG lasers. At the Etrat Institute of Technology, he worked on computer interfaces for industrial automotive robotic applications. His M.S. thesis was on development of a multisite physiologic recording system for investigation of neural assemblies, and his Ph.D. research was on developing a wireless microsystem for neural stimulating microprobes.

From 1994 to 1998, he worked part-time at the IDEA Inc., Tehran, where he participated in the development of the first modular patient care monitoring system in Iran. In December 1998, he founded Sabz-Negar Rayaneh Co. Ltd. to manufacture physiology and pharmacology research laboratory instruments. In the summer of 2002, he was with Advanced Bionics Inc., Sylmar, CA, working on the design of spinal-cord stimulators. He joined the faculty of North Carolina State University in August 2004, where he is currently an Assistant Professor in the Department of Electrical and Computer Engineering.

Dr. Ghovanloo has received awards in the operational category of the 40th and 41st DAC/ISSCC student design contest in 2003 and 2004, respectively. He is a member of Tau Beta Pi, the IEEE Solid-State Circuits Society, and biomedical engineering societies.



Khalil Najafi (S'84–M'86–SM'97–F'00) was born in 1958. He received the B.S., M.S., and the Ph.D. degrees, all in electrical engineering, from the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor. in 1980, 1981, and 1986 respectively.

From 1986–1988, he was employed as a Research Fellow, from 1988–1990 as an Assistant Research Scientist, from 1990–1993 as an Assistant Professor, from 1993–1998 as an Associate Professor, and since September 1998 as a Professor and the Director of the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan. His research interests include: micromachining technologies, micromachined sensors, actuators, and MEMS; analog integrated circuits; implantable biomedical microsystems; micropackaging; and low-power wireless sensing/actuating systems.

Dr. Najafi was awarded a National Science Foundation Young Investigator Award from 1992–1997, was the recipient of the Beatrice Winner Award for Editorial Excellence at the 1986 International Solid-State Circuits Conference, of the Paul Rappaport Award for co-authoring the Best Paper published in the IEEE TRANSACTIONS ON ELECTRON DEVICES, and of the Best Paper Award at ISSCC 1999. In 2003, he received the EECS Outstnding Achievement Award, in 2001 he received the Faculty recognition Award, and in 1994 the University of Michigan's "Henry Russel Award" for outstanding achievement and scholarship, and was selected as the "Professor of the Year" in 1993. In 1998, he was named the Arhtur F. Thurnau Professor for outstanding contributions to teaching and research, and received the College of Engineering's Research Excellence Award. He has been active in the field of solid-state sensors and actuators for more than 20 years, and has been involved in several conferences and workshops dealing with solid-state sensors and actuators, including the International Conference on Solid-State Sensors and Actuators, the Hilton-Head Solid-State Sensors and Actuators Workshop, and the IEEE/ASME Micro Electromechanical Systems (MEMS) Conference. He is the Editor for Solid-State Sensors for TRANSACTIONS ON ELECTRON DEVICES, an Associate Editor for the *Journal of Micromechanics and Microengineering* (Institute of Physics Publishing), and an editor for the *Journal of Sensors and Materials*. He also served as the Associate Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2000–2004, and the Associate Aditor for TRANSACTIONS ON BIOMEDICAL ENGINEERING from 1999–2000.