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# A Tri-State FSK Demodulator for Asynchronous Timing of High-Rate Stimulation Pulses in Wireless Implantable Microstimulators

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*Abstract*— **A tri-state FSK modulation protocol and demodulator circuit have been developed and explained in this paper for wireless data rates as high as the carrier frequency. This method is used for asynchronous timing of high-rate stimulation pulses in wireless implantable microstimulators to improve the timing resolution of the stimulation pulses from one data-frame period to only one carrier cycle period. The demodulator circuit is used in a 16-site wireless active stimulating microprobe fabricated in the University of Michigan 3-µm, 1-metal, 2-poly, N-epi, BiCMOS process, occupying 1.17 mm$^2$ of the probe active area. The FSK demodulator circuit is simulated up to 2.5 Mega bits per second (b/s) and tested up to 300 kb/s.**

*Keywords*— **Biomedical implant, CMOS, demodulator, FSK, inductive coupling, microstimulation, wireless**

## I. INTRODUCTION

Today, almost all biomedical implantable microelectronics are made wireless in order to reduce the risk of infection and patient discomfort as well as increase the robustness of the implanted device. Those implants with less power requirement such as pacemakers have an internal long lifetime battery [1]. The implants with high power requirements or extreme size constraints such as cochlear or visual implants need to be powered by an inductive link between two magnetically coupled coils to wirelessly transfer power and data from the external world to the implantable device [2]. However, this is not the only application of data and power transmission via inductive coupling. Radio-frequency identification (RFID), remote sensing, and MEMS are among other fields that can highly benefit from this technique. Achieving high power transmission efficiency, high data transmission bandwidth, coupling insensitivity, and small size are some of the challenges that one would face in the design of such systems.

In spite of extensive research, visual prostheses, which have a longer history than some commercialized devices such as deep brain and spinal cord stimulators, have not yet been widely utilized in patients as a cure for blindness [3]. The above challenges in general and the need for large amounts of data to simultaneously interface with a large number of neurons through multiple channels in particular, are the technological reasons behind this fact in addition to the natural complexity of the visual system. To operate a simple visual implant with a minimum functional resolution of only 32×32 pixels, each represented by a stimulating site [4], 10-bits for addressing, 6 to 8 bits for stimulation

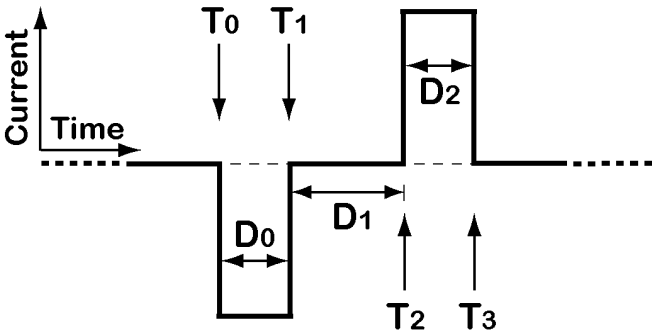


**Fig. 1.** A biphasic stimulation waveform and its timing information.

pulse amplitude levels, and 2 to 4 bits for polarity, parity-checking, and sequencing are needed. This suggests about 20-bits for site selection and amplitude information.

For the timing of stimulation pulses, three options have been proposed and called "basic", "single pulse", and "continuous pulse" modes by Jones and Normann in [5]. In the basic mode, every change in sites configuration is instructed to the implant by the external controller in real time. Therefore for a typical biphasic stimulation scheme, four successive 20-bit commands are needed to turn cathodic and anodic currents "on" and "off" at $T_{0\sim3}$, as shown in Fig. 1 by vertical arrows. In the single pulse mode, individual pulse timing is controlled by on-chip timers and a single command transfers timing information ($D_{0\sim2}$) in addition to amplitude and site selection to the implant prior to $T_0$. In the continuous pulse mode, a train of pulses is generated by a combination of on-chip timers and RAM to store timinig information on-chip. These three methods offer different levels of stimulation flexibility, bandwidth requirement, on-chip circuit size, and complexity. The best choice is determined by existing constraints in design of the implantable device.

Our goal is to develop an intracortical 1024-site wireless microstimulating 3D array for visual and auditory prostheses, consisting of up to 64 modules of 16-site wireless stimulating planar microprobes, called Interestim-3 and shown in Fig. 2, based on the University of Michigan micro-machined microelectrode array technology [6]. These probes are fabricated in-house in the MEMS-oriented 3-µm, 1-metal, 2-poly, N-epi, UM-BiCMOS process [7], whose large feature-size, single metal, and defect density limit the reasonable level of circuit complexity. However, it has the advantage of integrating the stimulating circuitry on the probe back-end. This solves part of the interconnection

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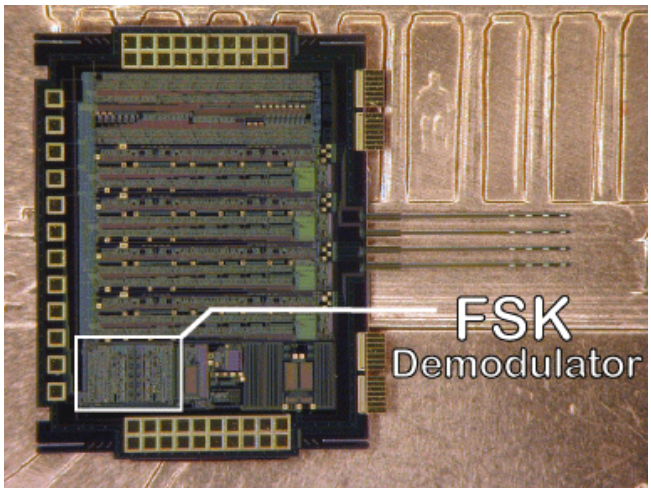


**Fig. 2.** Interestim-3, a 16-site wireless stimulating microprobe equipped with tri-state FSK demodulator on a US penny [6].

problem, which is the major cause of failure in cotrical implants with large number of stimulating sites, and reduces the overall implant size [2].

The basic timing mode provides the highest level of flexibilitily in generating any arbitrary waveform from any of the sites. In addition, the external controller takes care of the time keeping, thus there is no need for on-chip timers and their associated logic. This simplifies the implant circuitry significantly and consequently reduces its size in our 3-µm process. These advantages, however, come at the expense of larger required bandwidth. In view of the human-eye's natural bandwidth of 30 frames per second, scanning all 1024 sites at this rate needs a serial data bit stream of 1024-sites × 20-bits × 4-commands × 30-frames/sec = 2.46 Mb/s. Therefore, a high data-rate receiver circuitry that can establish an efficient wireless link between the implant and the external controller is highly needed.

We have developed several demodulator circuits based on a high-rate frequency shift keying (FSK) communication protocol for biomedical applications capable of achieving data rates as high as 67% of the carrier frequency. This demodulation method is based on measuring the period of each received carrier cycle, which is the information carrying entity in FSK modulation scheme [8]-[11]. All these demodulators also recover a constant frequency clock that is used to sample the serial data bits and send them into a shift register. Therefore, considering that the carrier frequency can be increased up to 20 MHz before the tissue losses become significant, achieving a data rate of 2.5 Mb/s is possible.

Synchronization between the implant and the external controller is accomplished by resetting the entire implant after detecting a unique data frame in the shift register followed by a continuous stream of constant-size back to back data frames. This method which is known as isochronous serial communication provides the highest net data rate compared to other serial communication techniques, and is used when a steady data stream is more important than its accuracy, as in video conferencing where small blips on the screen are acceptable. One drawback of combining basic timing mode with isochronous serial communication in visual prosthesis application is that the timing resolution of the stimulation pulses would be as long as a single data frame. In our visual implant example, a 20-bit data frame at 2.5 Mb/s limits the time resolution of stimulation pulses to 8 µs. This time resolution needs to be improved if we want to control and balance the injected charges in biphasic stimulations (Fig. 1) by both amplitude (AM) and pulse width modulation (PWM) [5].

In this paper we propose a tri-state FSK modulation protocol and demodulation circuit for asynchronous timing of high-rate stimulation pulses in wireless implantable microstimulators, which improve the timing resolution of the stimulation pulses from one data frame period to only one carrier cycle. Section II depicts the tri-state FSK modulation protocol. The new FSK demodulator circuit is described in section III. Section IV shows some of the measured results, followed by concluding remarks in section V.

## II. Tri-State FSK Modulation Protocol

In our phase coherent binary FSK protocol, logic "1" was assigned to a single cycle of the carrier $f_1$, logic "0" was assigned to two cycles of the carrier $f_0$, and $f_0$ was chosen twice in value as $f_1$ to achieve a constant data rate equal to $f_1$ and to extract a synchronizing constant frequency clock [8-10]. In this protocol the continuous flow of the data bit stream is essential to maintain the implant in-sync with the external transmitter even when the state of the system does not need to be changed. In other words, since the external parts of the system take care of all timing functions in the "basic" mode, Interestim-3 does not need a running clock at all times. Yet, the clock should be always running for the sake of synchronization.

In the tri-state asynchronous protocol, we choose three arbitrary frequencies in the desired band, assign logic "1" to $f_1$, logic "0" to $f_0$, and consider one frequency as the neutral frequency, $f_N$. The demodulator is designed such that when it receives neutral carrier cycles at $f_N$, it holds the prior status without generating any new clock cycles. Therefore, the entire implant freezes in its last state while still receiving power from the carrier. This asynchronous protocol has the following advantages in biomedical implant applications over its synchronous counterpart(s):

- Being able to freeze the implant for periods of time as small as one carrier cycle improves the timing resolution of the stimulation pulses from one data frame to $1/f_N$.
- Depending on the demodulator accuracy and the desired level of system robustness, in terms of bit error rate (BER) for example, the carrier frequencies can be chosen close to one another to occupy a narrower RF band without compromising the data rate.

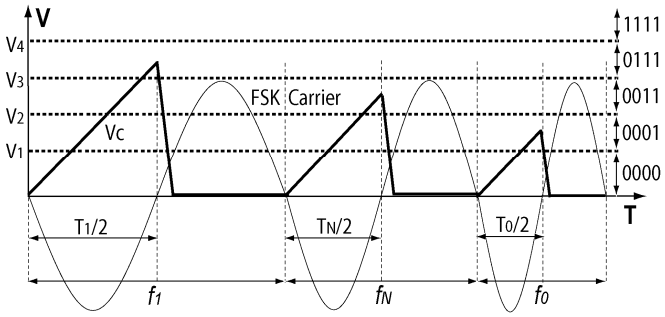


**Fig. 3.** Tri-state FSK protocol with $f_0 > f_N = (f_0+f_1)/2 > f_1$.

- Freezing the implant can save a significant amount of dynamic power, which would be wasted otherwise by running the system clock when the stimulator state does not need to be changed. This feature is more important in low power, low pulse rate applications such as deep brain stimulators.

In order to make the demodulator circuit design easier, we chose $f_0 > f_N = (f_0+f_1)/2 > f_1$ as shown in Fig. 3, although this does not necessarily need to be the case.

## III. Tri-State FSK Demodulator Circuit

Fig. 4a shows the FSK demodulator block diagram. Similar to [8], our demodulation procedure is based on measuring each carrier half cycle duration by synchronously charging a capacitor with a constant current source when the carrier is low and comparing its voltage with several reference levels. The clock recovery block is a cross-coupled differential pair which squares up the received sinusoidal carrier across the receiver LC tank ($CK_{in}$). $CK_{in}$ synchronizes an analog timer which converts the period of each carrier low half-cycle to a 4-bit thermometer code ($C_{1\sim4}$). Finally the thermometer code is decoded in a digital block to generate the demodulated serial data bit stream (Data_Out) and the recovered clock (Clock_Out). It also indicates the erroneous codes by asserting the error flag (Error_).

Fig. 4b shows a simplified schematic diagram of the synchronous analog timer (SAT). A resistor string generates four reference voltage levels ($V_{1\sim4}$) depending on the selected frequencies. When $CK_{in}$ is low, $S_1$ is closed and $S_2$ is open. Therefore, the capacitor C is charged and its voltage is compared with $V_{1\sim4}$ by four comparators, generating a thermometer code ($C_{1\sim4}$) proportional to the carrier half cycle period. Due to the tri-state FSK protocol in Fig. 3, the circuit parameters should be chosen such that they would satisfy the following inequality:

$$V_1 < \frac{I_C}{2f_0C} < V_2 < \frac{I_C}{2f_NC} < V_3 < \frac{I_C}{2f_1C} < V_4$$

Adjusting $V_2$ and $V_3$ at the center of the above ranges would maximize the demodulator robustness against transmitter frequency drifts (phase noise). $V_1$ and $V_4$ should be defined based on the minimum and maximum carrier frequencies in

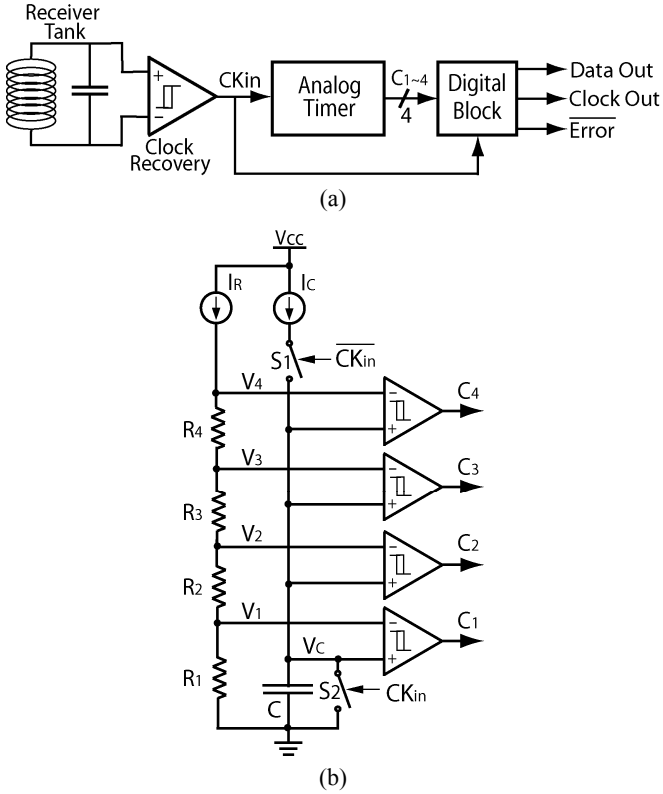


**Fig. 4.** (a) Tri-state FSK demodulator block diagram. (b) Synchronous analog timer schematic diagram.

the desired communication band, respectively, such that any received carrier cycle out of this range would be rejected. When $CK_{in}$ goes high, $S_2$ is closed to discharge the capacitor for detecting the next cycle, while $S_1$ is opened to save power.

The digital block samples the thermometer code at the rising edges of $CK_{in}$, while searching for the desired codes and changing the output data and clock signals according to Table 1. In this table, enabling the output clock means passing $CK_{in}$ to Clock_Out in order to allow the following shift register to sample the recovered data bit at $CK_{in}$ falling edges. During $f_N$ or any error cycles, Clock_Out is kept high, thus freezing the entire chip in its last state. The Error_ flag discriminates $f_N$ from too short, too long, and other erroneous cycles and can be used to trigger an action against these errors such as resetting the stimulator.

## IV. Measurement Results

Some of the internal node measured waveforms of the tri-state FSK demodulator can be seen in Fig 5a. From the top: the capacitor voltage ($V_C$), $C_2$ bit, Data_Out (inverted), and $CK_{in}$. In this experiment $CK_{in}$ is generated by a digital I/O card, while choosing $f_0$, $f_N$, and $f_1$ equal to 250, 215, and 180 kHz respectively. A symmetrical biphasic bipolar stimulation pulse generated by Interestim-3 (Fig. 2) [6], which is equipped with the tri-state FSK demodulator, is shown in

TABLE 1: THE DIGITAL BLOCK TRUTH TABLE

| $C_1 \sim C_4$ | Data_Out | Clock_Out | Error_ |
|---|---|---|---|
| 0111 | 1 | Enable | 1 |
| 0011 | No change | 1 | 1 |
| 0001 | 0 | Enable | 1 |
| All other combinations | X | 1 | 0 |

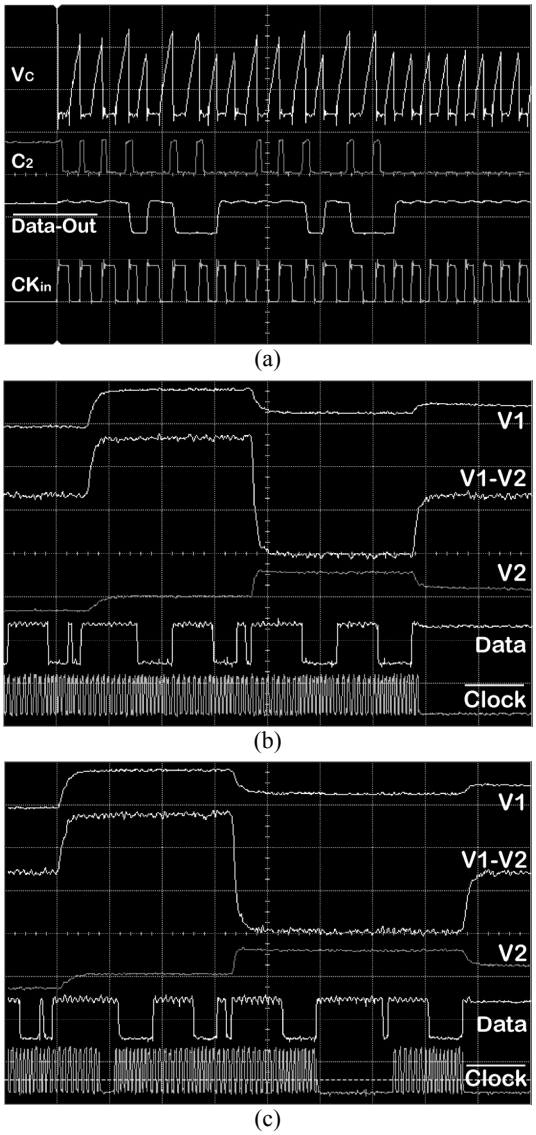


**Fig. 5.** (a) Measured waveforms from top: capacitor voltage, $C_2$ comparator output, demodulated data bit stream, squared up FSK carrier [10µs/div]. (b) A symmetrical bipolar-biphasic stimulation through a 10kΩ resistor. (c) A similar stimulation pulse made asymmetrical by adding neutral carrier cycles at $f_N$ to each phase.

in Fig. 5b. The lower two traces are the output clock (inverted) and data bit stream. The upper traces show single ended and differential stimulating site voltages, while a 10 kΩ resistor, resembling tissue, is connected between them. $V_1$-$V_2$ is proportional to the bipolar-biphasic current that passes through the tissue. Fig. 5c shows a similar pulse that is made asymmetrical by adding different numbers of neutral cycles at $f_N$ to both cathodic and anodic phases.

## V. CONCLUSION

We have developed a new tri-state FSK modulation protocol and demodulator circuit for wireless data rates as high as the carrier frequency. This method is used for asynchronous timing of the high-rate stimulation pulses in wireless implantable microstimulators to improve the timing resolution of the stimulation pulses from one data frame period to only one carrier cycle. The demodulator circuit is used in a 16-site wireless active stimulating microprobe fabricated in the University of Michigan 3-µm, 1M/2P, N-epi, BiCMOS process, occupying 1.17 $mm^2$ of the probe active area. The FSK demodulator circuit is simulated up to 2.5 Mb/s and tested up to 300 kb/s. We are currently working on a new version of this demodulator with higher data rates to be implemented in a foundry CMOS process.

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