Design and Testing of a Photosensor for Intraocular Prostheses

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Abstract

This paper shows the design and testing of a photosensor chip for intraocular prostheses. The chip has 4 pixel cells that each detect light and indicate it's detection by sending a current pulse to neurons in the retina's outer plexiform via the RTI stimulator. The design of the pixel cells are examined first. This is followed by a discussion on the operating modes in which the pixel cells can be used. Procedures for wiring the chip are also discussed. The final part of the paper deals with the testing of the photosensor chip.

1 Basics of the Photosensor Chip

The purpose of the photosensor chip is to emulate some of the functions carried out by the human retina. Like the human retina, the chip will check for the presence of light and indicate it's presence with a current pulse to neurons in the outer plexiform. The light checking and current pulse generation will be performed by light detecting pixel cells located on the chip. There are 4 of these pixel cells, one in each corner of the chip, that act independently of each other. To coordinate the operation of these pixel cells, the chip also has some control logic. This logic allows two operation modes for the pixel cells, a manual mode and an automatic mode. These operating modes make the photosensor chip easier to use while permitting much functional versatility.

This paper describes the chip design fabricated in 2.0μm CMOS, shows how to use the chip, and evaluates it's performance. First the design of the chip's 4 pixel cells will be discussed. This will be followed by discussion of the photosensor chip's two operating modes. Instruction on wiring the chip are then given. The final part of this paper deals with the photosensor chip's tested performance.

Appendices also follow this paper that act as a quick reference guide when using the photosensor chip. Appendix A gives the general specifications of the chip, Appendix B shows the chip's possible manual mode settings, and Appendix C shows a wiring diagram of both the packaged and unpackaged versions of the photosensor chip.

2 Pixel Cell

The photosensor chip's 4 pixel cells detect the presence of light and output a current pulse to neurons in the retina's outer plexiform when light is detected. Each pixel cell is comprised of a photo detector, a sense amp, some control logic, and a current output circuit. A logic block diagram for the pixel cell appears below in Figure 1. A pixel cell works by first detecting light with its photo detector. After detecting light, the photo detector outputs a voltage whose magnitude is relative to the intensity of the light. This output voltage is then compared by the sense amp to some threshold voltage, V_{thresh}, set off chip. If the output voltage created by the light is greater than V_{thresh}, the sense amp indicates that the pixel cell may output a current pulse to the neurons. This indication by the sense amp is then combined with various control and clock lines in the control logic. The output of the control logic then determines if the current output stage can output a current pulse to the neurons. The control logic also dictates the type of current pulse the current output stage creates. The photo detector, the current pulse created for the neurons, and the current output stage will now be examined.

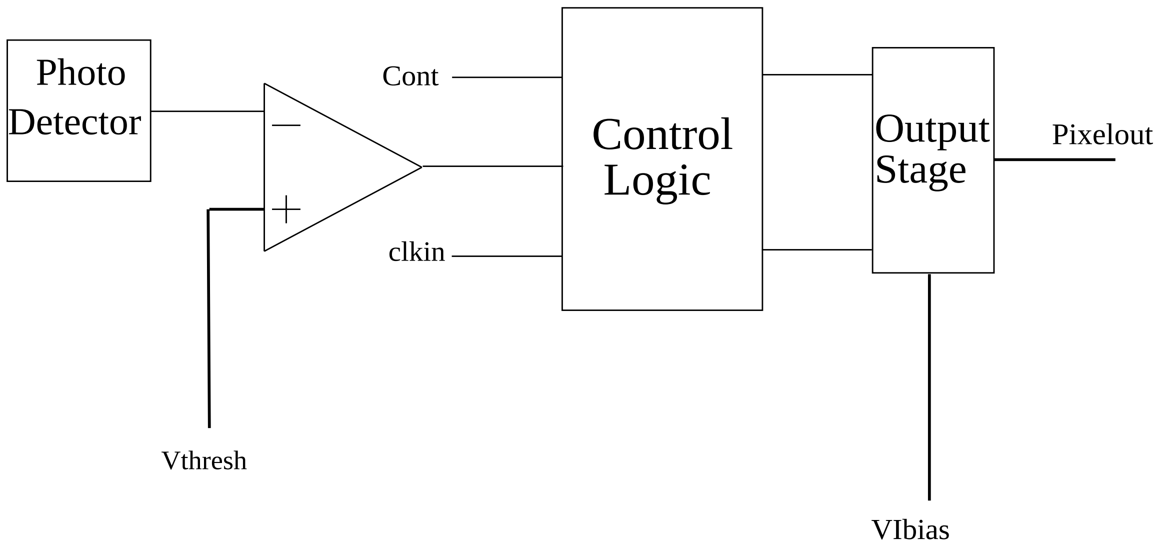


Figure 1: Logic Block Diagram of Pixel Cell

A schematic for the photo detector appears below in Figure 2. The design, similar to one created by Carver Mead, is simply one npn transistor and two diodes. The npn transistor creates a current proportional to the light hitting the transistor's base. This current is then converted to a voltage by the diodes and this voltage is the output of the detector. The more intense the light is on the npn transistor, the higher the output voltage. The photo detector's sensitivity to light is controlled by the size of the npn transistor. The size and topology for this transistor are shown in Figure 3. The photo detector also works with a pnp transistor, demonstrated in an earlier photosensor chip designed at NCSU by C. Thomas Gray.

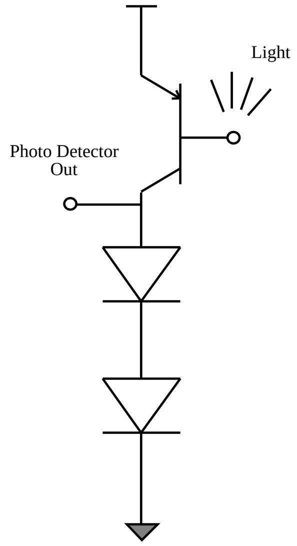


Figure 2: Schematic for Photo Detector

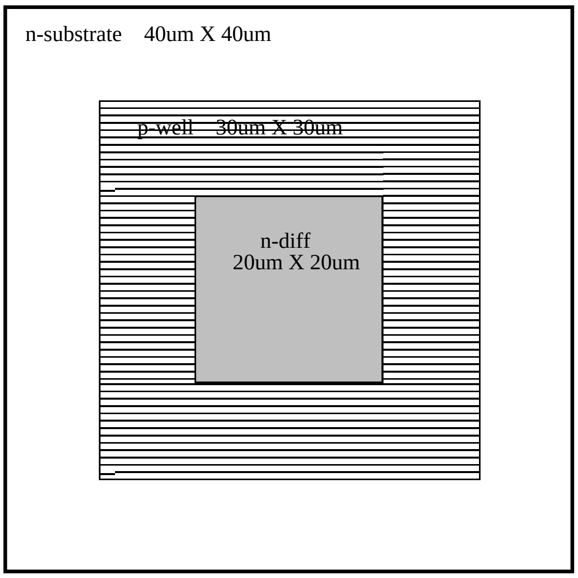


Figure 3: Topology of NPN Transistor with Sizes

The current pulse output generated by a pixel cell is similar to the pulse generated in the human retina. This pulse delivers charge to neurons in the retina's outer plexiform to indicate light was detected by the pixel cell. After indicating the light detection, this charge must be removed since excess charge could damage the neurons. The current pulse must, therefore, be a positive current that delivers charge to the neurons followed by a negative current to then discharge the neurons. The plot in Figure 4 shows what the current pulse will look like. To keep the neurons charge neutral, both areas under the plot's positive and negative curves must equal. These areas are determined by the magnitude and duration of both the positive and negative currents. Control of these magnitudes and durations are handled by a pixel cell's current output stage and control logic.

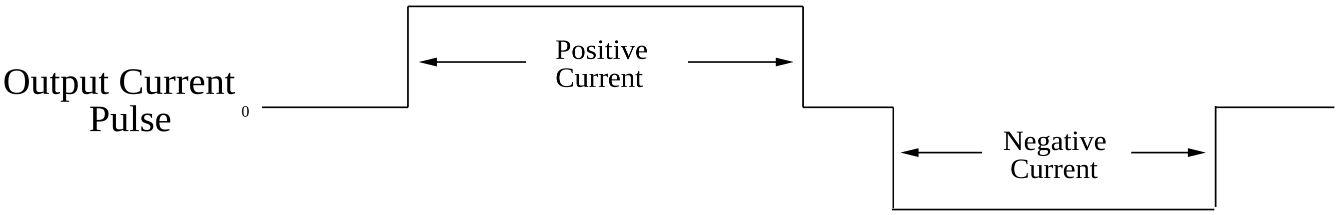


Figure 4: Output Pulse Created by Pixel Cell Current Output Stage

The current output stage was designed to output a current pulse, shown in Figure 4, to a 1KΩ load tied to GND. The schematic for the this output stage appears below in Figure 5. The output stage consists of a bias voltage, 2 current mirrors, and 2 pass gates. The bias voltage and current mirrors control the magnitude of the positive and negative currents. By increasing the bias voltage, V_{Ibias}, the magnitudes of both currents increase. The current mirrors try to equalize the magnitudes of the positive and negative currents but cannot keep these magnitudes equal over the entire range of V_{Ibias}. It is necessary, therefore, to control the durations of each of these currents to prevent charge from building up on the neurons. Control of these durations is handled by the 2 pass gates.

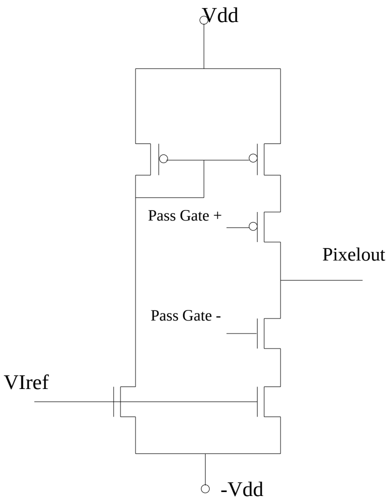


Figure 5: Current Output Stage of Pixel Cell

The pass gates in the current output stage control both when an output pulse occurs and the duration of an output pulse's positive and negative currents. When neither pass gate is active, the output stage is in a high impedance state and no output pulse occurs. The stage's output node sits at GND since no current can flow from the output to its 1KΩ load tied to GND. For current to flow from the output stage, one of its pass gates must be active. Only one of the pass gates can be active at one time, and which pass gate is active determines whether the output current is positive or negative. Also, the time a pass gate is active determines the duration of the gate's associated output current. The pass gate's time active is controlled by a 3 level clock signal, which is generated off-chip, applied to the photosensor chip's *clkin* pin. Figure 6 shows this clock signal with the output current pulse it creates. The time the clock signal is high (3 V) controls the output pulse's positive current duration. The duration of the negative current is determined by the time the clock signal is low (-3 V). When the clock signal is at the mid-level voltage (GND), both pass gates are inactive and no output current occurs. Both pass gates can also be made inactive by blocking the clock signal in the control logic preceding the current output stage. Using various control lines to block the clock signal in the control logic, the output stage would not output any current pulses and the entire pixel cell would then effectively be disabled. The setting of the control lines to disable specific pixel cells is discussed in the next section on photosensor chip operating modes.

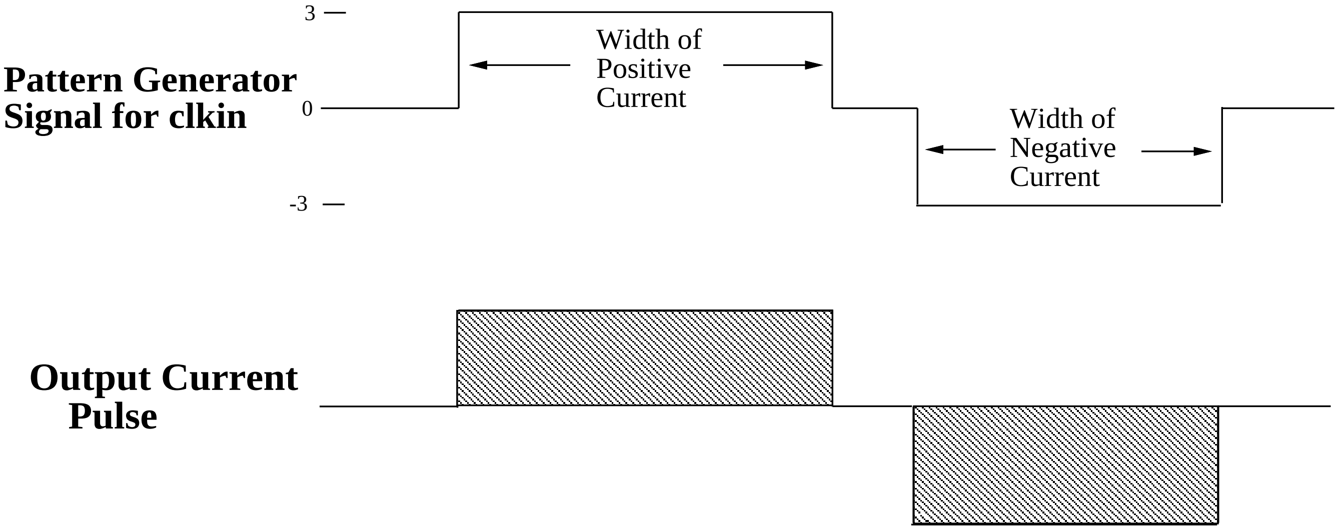


Figure 6: Clock Signal Generated by Pattern Generator and Current Output Pulse

3 Operating Modes for the Photosensor Chip

Only enabled pixel cells can output current pulses when detecting light, and the photosensor chip controls which pixel cells are enabled through two operating modes. The two modes are manual mode and automatic mode with the $auto/\overline{man}$ pin specifying the chip's current mode of operation. Driving the $auto/\overline{man}$ pin low puts the photosensor chip in manual mode and only one specified combination of pixel cells can be active. Automatic mode is entered by setting the $auto/\overline{man}$ pin high. This mode allows the chip to cycle through 8 different combinations of active pixel cells. The use of each of these modes will now be explained.

3.1 Manual Mode

The manual mode is the simplest operating mode but it allows only one combination of pixel cells to be enabled. To control which pixel cells are enabled, five pins, *m1*-*m5*, are used. These pins can be set to enable either a single pixel cell, pairs, triples, or all 4 pixel cells at once. The settings of pins *m1*-*m5* that enable the various pixel cell combinations appear in Appendix B.

3.2 Automatic Mode

The automatic mode cycles the photosensor chip through 8 different pixel cell combinations. The heart of this mode is an 8 state, state machine with each state representing one of the desired pixel cell combinations through which the photosensor chip cycles. Each state has 4 bits with each bit associated with one of the pixel cells. A set bit in a state enables its associated pixel cell when the state machine is in that state. The 4 enabling bits in each of the 8 states are set by the 32 bit shift register. Each bit of the shift register acts as one of the state machine's enabling bits. Entering a 32 bit pattern into the shift register will set the combination of pixel cells through which the state machine will cycle. Instructions on using the state machine and loading shift register will now be given.

The state machine is controlled by the chip's reset, *s8rst*, and clock signal line, *clkin*. Setting *s8rst* low for one clock period resets the state machine to state 1. When *s8rst* is high, the state machine will continually cycle through its 8 states. State changes are caused by the same clock signal that controls the pixel cells' output signals, *clkin* (Figure 6). Transitions of *clkin* from low voltage (-3V) to mid voltage (GND) cause state changes to occur. After changing states, the shift register bits associated with the new state are checked and appropriate pixel cells are enabled.

Loading of the 32 bit shift register is done using the *srin* and *srclk* pins. The bits to place in the shift register are entered on *srin*. Pixel 4's 8 enabling bits are entered first followed by the bits for Pixel 3, Pixel 2, and finally Pixel 1. For each pixel cell, it's 8 enabling bits are entered in reverse order. This means the enabling bit for a pixel cell in state 8 is entered first followed by the pixel cell's enabling bits for states 7 down to 1. The *srclk* line clocks the bits on *srin* into the shift register. The signal for *srclk* is a normal clock signal (-3V to 3V) and clocking occurs on this signal's falling edge.

4 Wiring of the Photosensor Chip

This section shows how the photosensor chip is wired for use. It first shows the input and output pins that are wired regardless of the chip's mode of operation. Next, wiring for the specific operation modes, manual and automatic, is discussed. The final part of this section deals with hardwiring an unpackaged die of the photosensor chip. The pin diagram for both the packaged and unpackaged versions of the photosensor chip appear in Appendix C.

The photosensor chip's input pins used in both operation modes are shown below. Each input pin is listed along with its required connection.

Vdd	3V
-*Vdd*	-3V
GND	0V
V_{thresh}	-3V to 3V - determines amount of light required to activate photo detectors in all the 4 pixel cells
V_{Iref}	-3V to 3V - determines the magnitude of the output pulses created by all 4 pixel cells
clkin	- 3 level clock signal (shown in Figure 6) generated by an off chip, signal generator
$auto/\overline{man}$	- determines mode of operation, 3V auto mode, -3V manual mode

The chip's output pins are the same for both modes of operation. The outputs consist of the 4 pixel cell outputs (*pixelout1-4*) and the output of pixel cell 2's photo detector, *pdout*. The output of each of the four pixel cells indicate when a pixel cell detects light, and each output will be connected to 1KΩ resistors tied to GND. The output *pdout* indicates the intensity of the light detected by pixel cell 2's photo detector.

When using manual mode, the only pins used in addition to the ones previously listed are the 5 pins, *m1-5*. These pins set the chip to the pixel cell combinations listed in Appendix B. Each of these pins would connect to switches passing logic levels of -3V or 3V.

In automatic mode, the additional connections are *srin*, *srclk*, and *s8rst*. These pins set up the chip's automatic mode as described in the section on the automatic mode. The 3 automatic mode pins are each connected to switches passing logic levels of -3V or 3V.

The photosensor chip's design also permits hardwiring of an unpackaged chip die to a set, pixel cell combination. Hardwiring would configure a die to a desired manual mode, pixel cell combination and not allow the die to assume any other combination. The die would also have V_{thresh} and V_{Iref} hardwired to fixed voltages generated on the die. Though a hardwired die is less flexible to use, it would require fewer external connections for control. Having fewer external connections eases placement of the die in a human eye since fewer wires will have to pass through the eye. Instructions for hardwiring the die will now be shown.

Hardwiring is accomplished by bonding certain die pads to other, adjacent pads. First, the $auto/\overline{man}$, *srin*, *srclk*, and *s8rst* pads are each be bonded to an adjacent -*Vdd* pad so that the photosensor die is permanently in manual mode with none of the automatic mode pads floating. Both the V_{thresh} and V_{Iref} pads are bonded to one of the bias voltage pads adjacent to them. The voltages on the bias pads on either side of the V_{thresh} and V_{Iref} pads are created by on-chip voltage dividers. The 5 pads *m1-5* are then bonded to adjacent pads to permanently set the die's enabled, pixel cell combination. Each of these 5 pads is between a pair of pads at both logic levels (-3V and 3V), so the die can be bonded into any of the pixel cell combinations shown in Appendix B. Once hardwired, the die only requires external connections to *Vdd*, -*Vdd*, *GND*, and *clkin*.

5 Testing of the Photosensor Chip

There were three areas of testing for the photosensor chip. First the chip was checked to see if it was functionally correct. Tests were then done to determine the relationship between the bias voltage, V_{Iref}, and the magnitudes of the output currents generated by the output stage. The third testing area has not been completed but would show the effects of specific light intensities on the output voltage of a photo detector. The completed functional tests and output stage tests will now be discussed.

5.1 Functional Tests

The photosensor chip was tested in both manual and automatic modes and is functionally correct. Simulations show the chip to work at up to 10MHz, but the chip was tested at speeds no faster than 1KHz. This slower clock rate is the speed at which the chip has to operate in the human eye.

5.2 Current Output Stage Tests

The current output stages of the pixel cells were tested to determine the effect of V_{Iref} on output current. The bias voltage V_{Iref} was swept rail to rail and the magnitudes of the positive and negative currents generated by the output stage were measured. The results of these tests appear in Figure 7. The graph in Figure 7 shows how the magnitudes of the currents change over the entire range of V_{Iref}. This graph shows that the magnitudes of the two currents are nearly equal at 100μA but become increasingly unequal as the magnitudes increase. Since the magnitudes are usually unequal, control of each current's duration is critical to prevent damage to the neurons in the retina's outer plexiform.

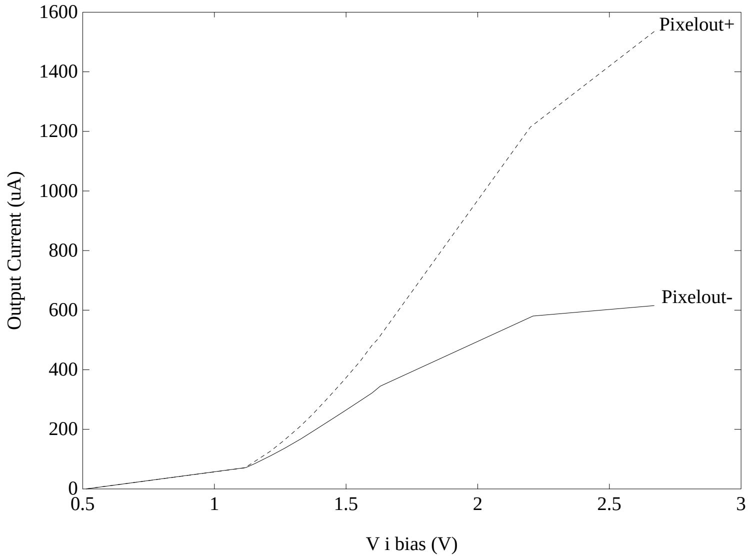


Figure 7: Effect of V_{Iref} on Output Currents

6 Conclusion

A photosensor chip was designed to emulate parts of the human retina. The chip is capable of detecting light and indicates light detection by sending a current pulse to neurons in the retina's outer plexiform. The tests performed on the chip and its current output stages show everything working as expected. Tests on the effects of light on the chip's photo detectors still need to be completed.

A Specifications of the Photosensor Chip Die

The sizes for the die and various components appear below.

size of die	- 2250μm X 2220μm
size of pixel cell	- 145μm X 225μm
size of photo detector	- 20μm X 20μm
size of pad	- 102μm X 102μm

B Settings for Manual Mode Pixel Cell Combinations

Switches m1-5 control the pixel cells in manual mode.

Single Pixel Cells (m5 m4)

Switch Setting	Pixel Cells 1	2	3	4
$\overline{m1}$ $\overline{m2}$	on	-	-	-
m1 $\overline{m2}$	-	on	-	-
$\overline{m1}$ $m2$	-	-	on	-
m1 m2	-	-	-	on

Pixel Cell Pairs (m5 $\overline{m4}$)

Switch Setting	Pixel Cells 1	2	3	4
m1 $\overline{m2}$ $\overline{m3}$	on	on	-	-
$\overline{m1}$ m2 $\overline{m3}$	on	-	on	-
$\overline{m1}$ $\overline{m2}$ m3	on	-	-	on
m1 $\overline{m2}$ m3	-	on	on	-
m1 m2 m3	-	on	-	on
$\overline{m1}$ m2 m3	-	-	on	on

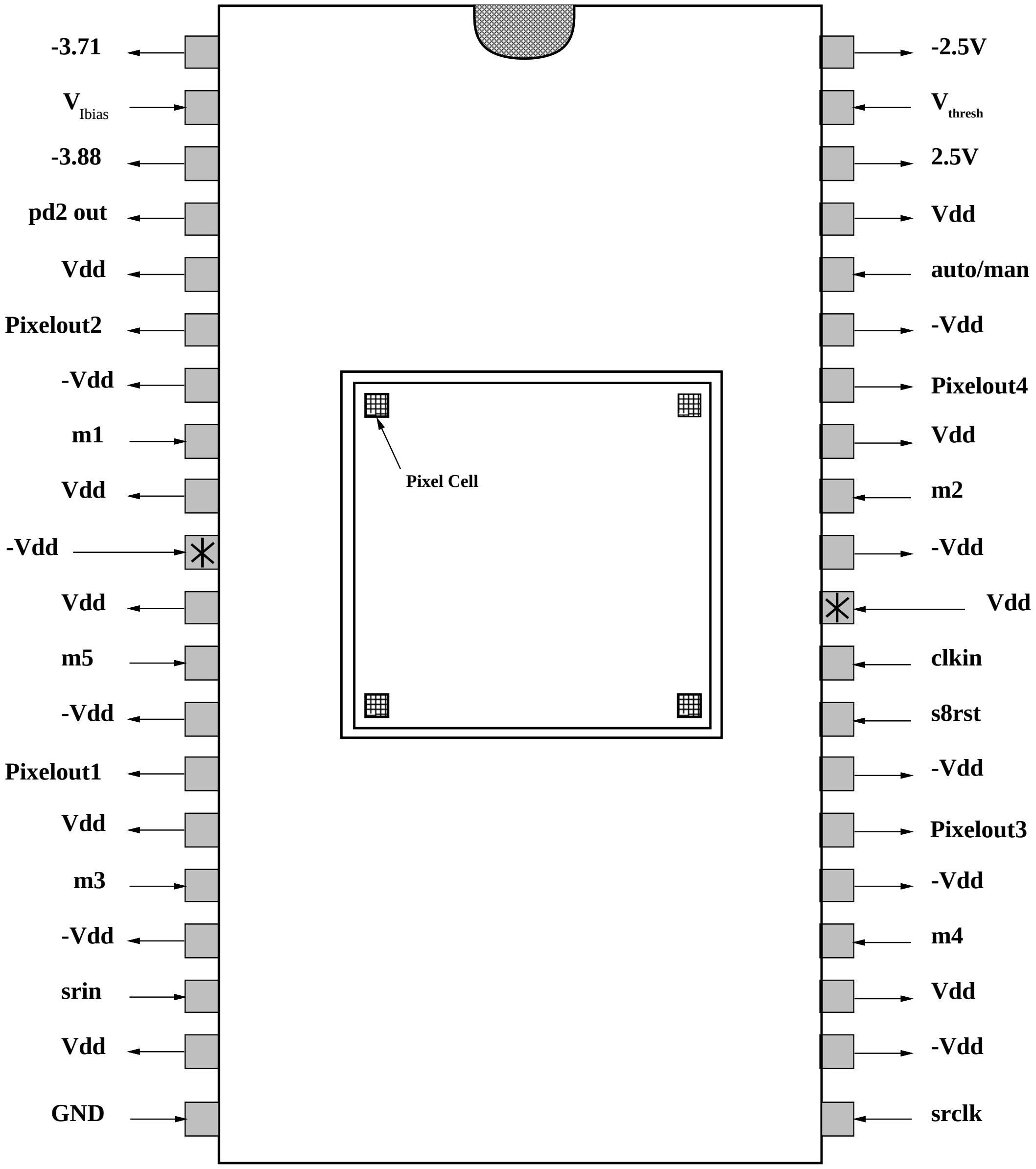
Pixel Cell Triples ($\overline{m5}$ m4 $\overline{m3}$)

Switch Setting	Pixel Cells 1	2	3	4
$\overline{m1}$ $\overline{m2}$	on	on	on	-
$m1$ $\overline{m2}$	-	on	on	on
$\overline{m1}$ $m2$	on	-	on	on
m1 m2	on	on	-	on

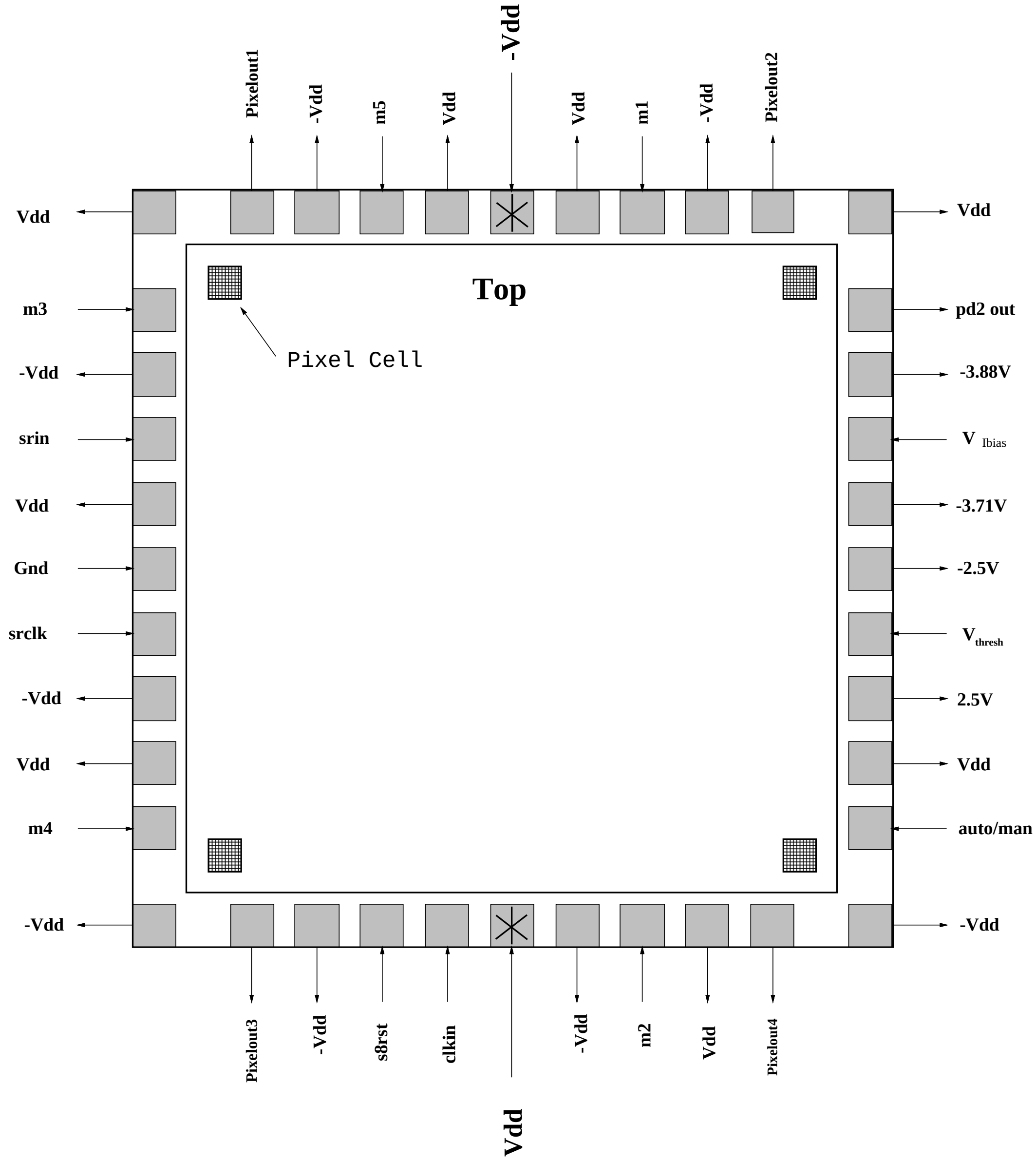
All pixel cells are off in setting ($\overline{m5}$ $\overline{m4}$ $\overline{m3}$ $\overline{m2}$ $\overline{m1}$)

All pixel cells are on in setting ($\overline{m5}$ $\overline{m4}$ m3 $\overline{m2}$ m1)

C Pin Diagrams for Packaged and Unpackaged Photosensor Chips



NOTE: The chip's power lines, Vdd and -Vdd, are connected to the center, starred pins.



NOTE: The die's power lines, Vdd and -Vdd, are connected to the center, starred pads.