CAD Tools for the Automated Design of High Speed Multichip Modules

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Abstract

Future multichip modules will contain over 10,000 connections, many of which will be clocked at frequencies between 100MHz and 10GHz. Current design approaches to high speed interconnect are based around simulation studies carried out on a SPICE-like tool, employing RLGC models. From these simulation studies, design rules are formed. There are a number of limitations with this approach: First, design by analysis is time consuming, does not necessarily lead to insight and results in conservative designs. Second, the characteristic impedance for a multichip module interconnect varies considerably with frequency, making SPICE-like calculations limited.

In this paper we address these limitations. A design methodology based on synthesis, rather than on analysis, is proposed. This design methodology has been implemented in a placement tool, Panda. The nature of MCM characteristic impedance is discussed and, a simulator suitable for MCMs, Transim, is presented.

1 Introduction

The current industrial approach to high speed interconnect design is illustrated in Figure 1. It is based around a number of concepts, including the following:

1. The determination of characteristic impedance $Z_0 = \sqrt{\frac{L_0}{C_0}}$, where C_0 is calculated by finite element analysis and $L_0 = \frac{c}{C_0(\text{free space})}$ where c is the speed of light in a vacuum, and C_0(free space) is the capacitance without a dieletric.

2. The lines are assumed to be low-loss over the frequency range of interest, and this loss is assumed to be fixed.

3. The number of critical nets is small enough that they can be analyzed individually by hand simulation using an RLGC model in a SPICE-like tool;

4. Physical design rules (length, spacing) for nets are fixed in advance through simulation of a number of cases.

Future systems will have faster edge times, tighter electrical requirements, and larger numbers of delay-critical nets. Future MCMs may contain 25 ICs with over 1,000 I/Os per IC [13] resulting in a requirement to route

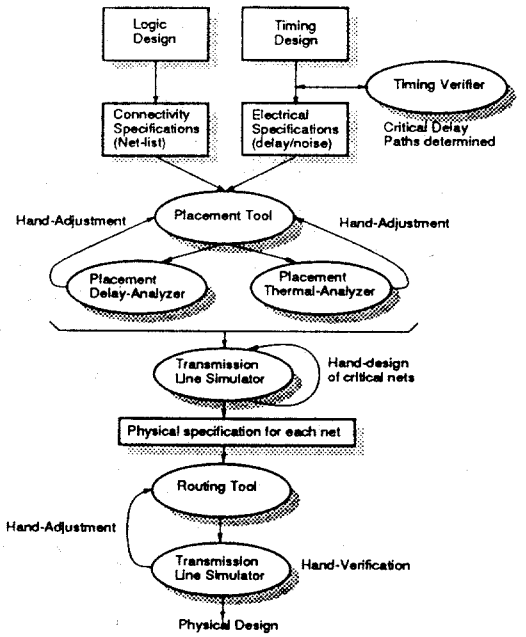


Figure 1: Current design process for High Speed Systems.

over 10,000 nets. With typically over 10% of these nets being critical, design through simulation will become both time-consuming and error-prone.

Instead a more highly automated process is proposed (Figure 2.) This proposed tool set displays a number of features that make it suitable for GHz-frequency designs:

- The placement tool is attached to a delay model base. This delay model base will automatically compare specified delay with estimated delay as a result of a particular placement, ensuring the placement meets specification.
- The routing tool will be guided by the delay and noise model base, which will be used to generate the physical design rules for each net as required. These models will result in estimates only of the allowed physical design space. By making the models conservative, the resulting routes should still be able to meet the electrical design specifications. It should not lead to the same degree of over-design that the current CAD process does.
- The transmission line simulator will be used to automatically verify each net and and the router will adjust each net as required.

Two of these tools have been implemented. These will be described in this paper:

1. The simulator.
2. The IC placement tool.

Before proceeding with this, the nature of characteristic impedance in MCMs will be discussed.

2 Characteristic Impedance of MCMs

Transmission Lines are characterized by their characteristic impedance Z_0, their propagation constant $\gamma = \alpha + j\beta$, and their equivalent distributed circuit parameters R, L, G, and C. These are related by:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (\Omega) \tag{1}$$

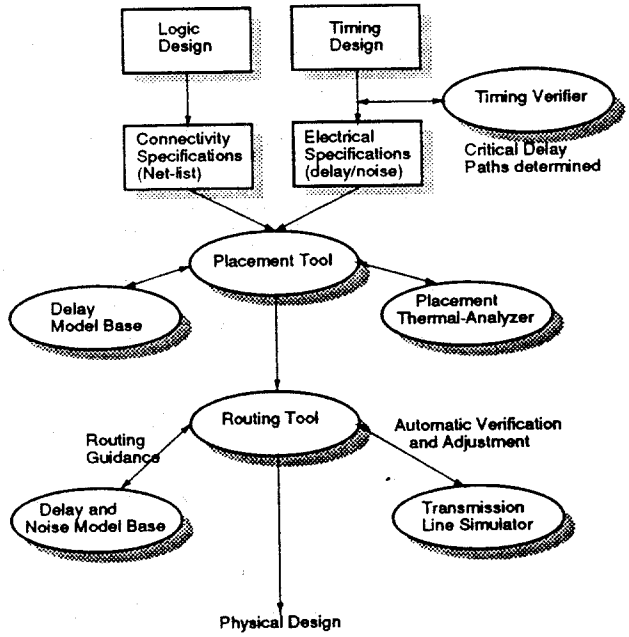


Figure 2: Proposed design process for High Speed Systems.

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2}$$

$$\mu_p = \frac{\omega}{\beta} \quad (m^{-1}) \tag{3}$$

The conventional approach to determining these parameters for say a PCB connection (microstrip or stripline) is as follows:

1. Calculate, using a field-solver or an empirically-derived expression, C with the dieletric present.
2. Calculate C_0 for the line with no dieletric present. Assume that all of the current flows on the outside of the conductor and thus $L = \mu\epsilon/C_0$.
3. Calculate R at a fixed frequency, assuming that it is flowing in a skin of a certain depth.
4. Assume $R \ll \omega L$ and calculate $Z_0 = \sqrt{L/C}$.
5. Calculate the losses, $\alpha = R/(2Z_0)$
6. Assume that the phase velocity $v_{ph} = \omega/\beta$ is constant.

This approach neglects a number of effects that are important for multichip module interconnect:

1. The current is distributed throughout the entire cross-section of the conductor until a frequency, of about 1GHz, is reached, at which the skin depth becomes comparable to the strip thickness. Below this frequency, the inductance is increased by the amount of the internal inductance of the conductor, and the resistance is close to its DC value. Above this frequency R increases dramatically due to the skin effect.
2. R is high for MCM interconnect, so the common assumption $R \ll \omega L$ may not be true in the frequency range of interest.

Thus R and L are actually frequency dependent parameters. One method to calculate these parameters was developed by Weeks [14] and implemented at MCNC [10]. This method was applied to the buried microstrip conductor shown

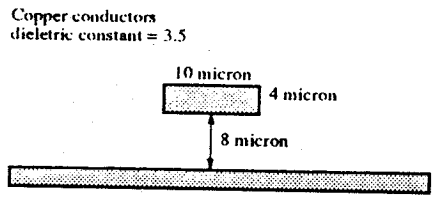


Figure 3: Microstrip Cross-Section analyzed.

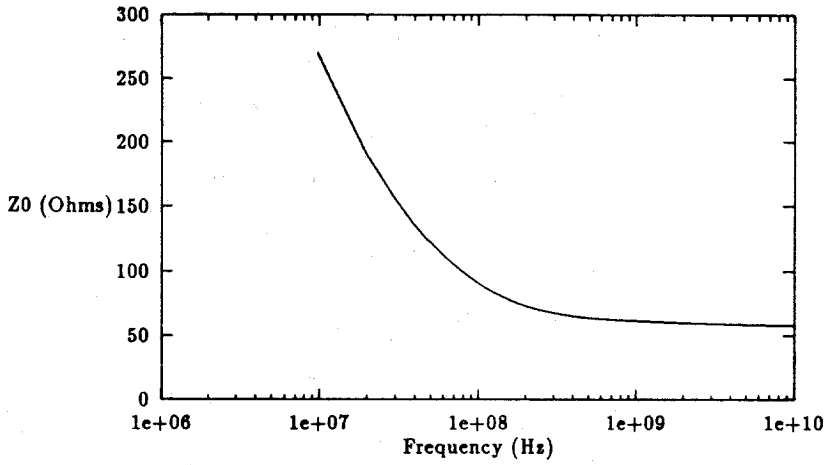


Figure 4: Characteristic Impedance vs. Frequency.

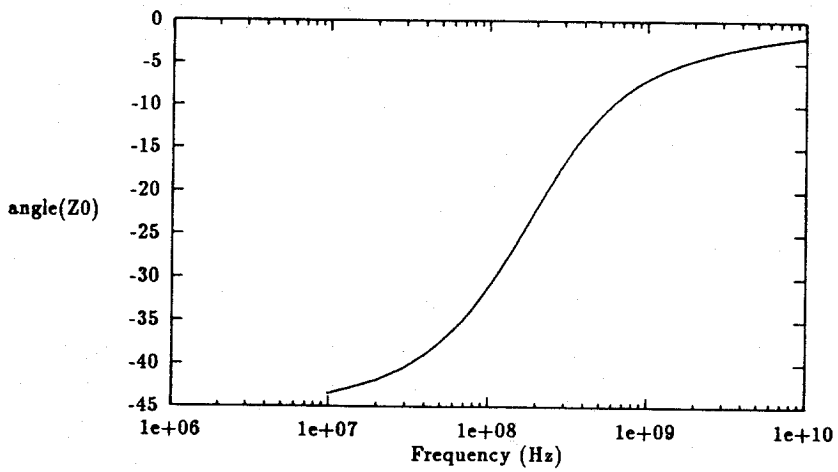


Figure 5: Characteristic Impedance angle vs. Frequency.

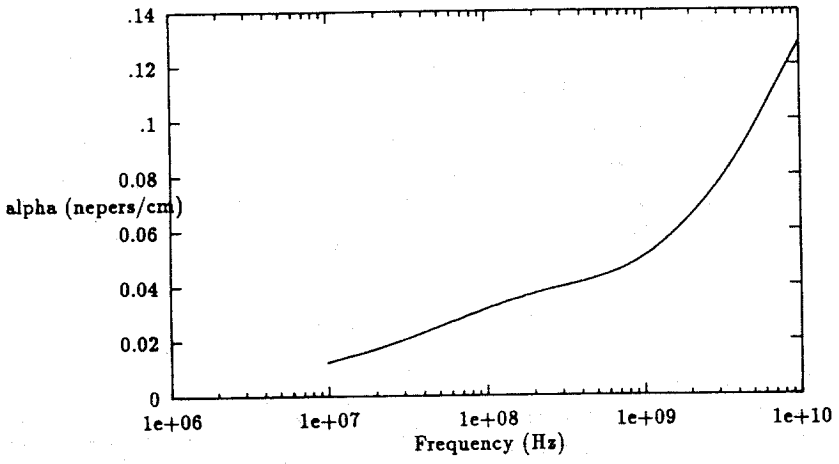


Figure 6: Losses vs. Frequency.

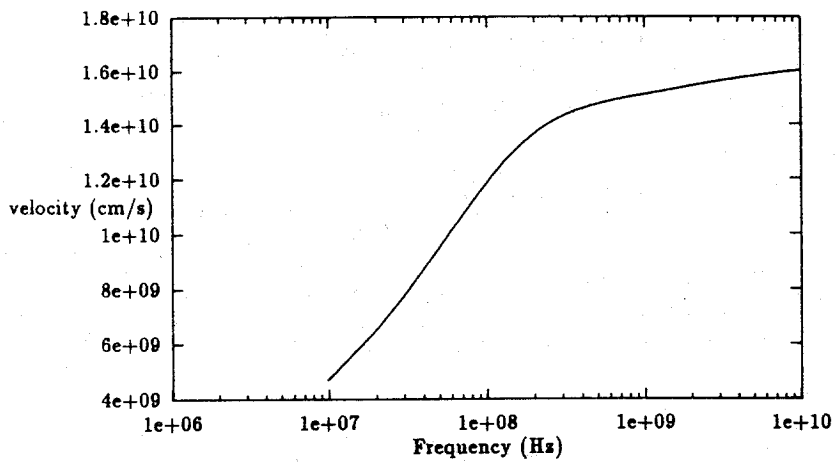


Figure 7: Phase Velocity vs. Frequency.

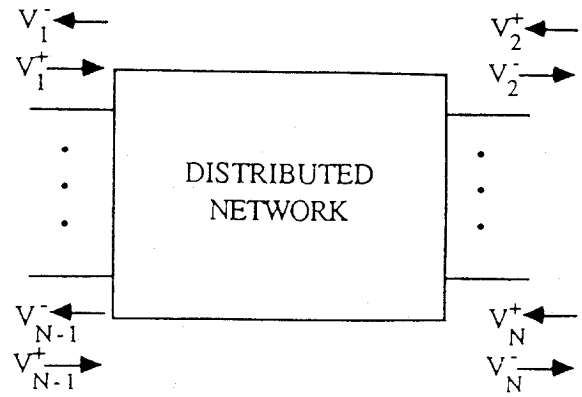


Figure 8: N port distributed network.

in Figure 3. The results are plotted in Figures 4 to 7. It can be seen that the combination of these effects are important. For frequencies below 100–200MHz, the phase velocity is low as R dominates over L. For frequencies in the range between 100MHz and 2GHz, the effect of including internal inductance is to increase Z_0 by up to 5%. Above 1GHz, the skin effect causes the resistance, R, and thus the losses, α, to increase. Thus the values of all the parameters of importance vary substantially with frequency. As the spectrum of a typical digital pulse of width T_W has significant components that go out to frequencies of $5/T_W$ and beyond, it is essential to be able to simulate these lines using frequency domain parameter descriptions.

As most interconnection simulators allow only frequency-invariant component values, a new interconnection simulator, Transim, has been developed at North Carolina State University.

3 Interconnection Simulator

The fundamental difficulty encountered in integrating transmission line simulation in a transient circuit simulator arises because circuits containing nonlinear devices or time dependent characteristics must be characterized in the time domain while transmission lines with loss, dispersion, and interconnect discontinuities are best simulated in the frequency domain.

Our approach is similar in some respects to that of Djordjevic et al [6], expect that where Djordjevic et al use admittance (Y) parameters to characterize the frequency dependent network, we use the scattering (S) parameters. As the S parameters vary only between -1 and +1, we overcome the dynamic range problems with Djordjevic's approach.

We derive a Green's function from the frequency-domain S parameters and use this to develop a method for analyzing an arbitrarily complex transmission line network terminated in nonlinear loads. Implementation of the technique is discussed and it is verified by comparing it with measured results.

3.1 Development of Method

S parameters of a transmission line system describe the relative amplitude and phase of the forward and backward traveling waves at each port and at each frequency on a transmission line of, here, characteristic impedance Z_m. For complete generality the transmission lines can be of infinitesimal length as in Figure 8.

Here V_j^+ and V_j^- are the forward and backward traveling waves respectively at the j th port and a frequency-domain S parameter is just the ratio of the backward traveling wave to the forward traveling wave, $S_{ij}(\omega) = V_i^-(\omega)/V_j^+(\omega)$. Thus each S parameter has a direct physical relationship with a reflection or coupling process. Each time-domain S parameter (being the Fourier transform of the corresponding frequency-domain S parameter) is then the response of a backward traveling wave with respect to an impulse forward traveling wave at one of the ports of the network with all ports terminated in the reference impedance, Z_m, of the S parameters, i.e. $S_{ij}(t) = V_i^-(t)/V_j^+(0)$.

Integration into a transient circuit simulator requires that the description of the transmission line system be in terms of total voltages rather than traveling wave components. This can be achieved by terminating each port in

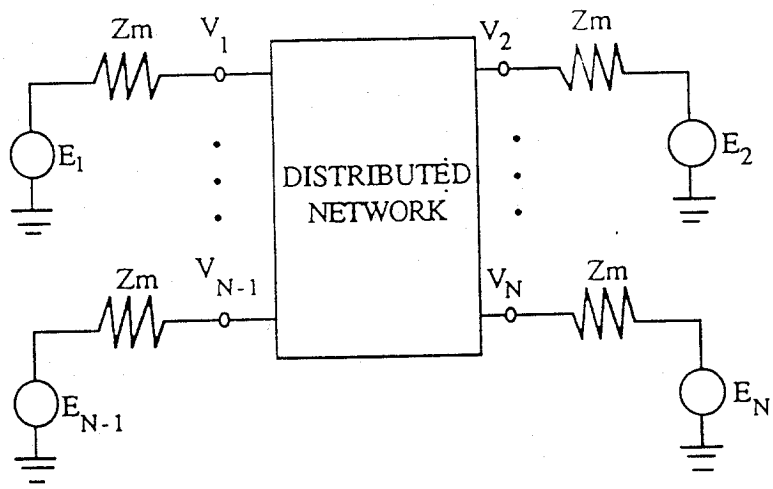


Figure 9: N port distributed network with reference impedance termination and arbitrary sources.

its reference impedance so ensuring that there are no reflections at the ports of the distributed network. This is illustrated by considering the multiport transmission line network of Figure 9 with ports terminated in Thevenin equivalent loads (or sources) each with reference impedance Z_m. Now the total transient response of any linear network to voltage sources at the ports of the network can be determined by convolving in time these voltages with the Dirac impulse voltage responses at each external port of the network. More explicitly, and referring to Figure 9, the total transient response at port i of a transmission line system to a total voltage $E_j(t)$ $(= V_j^+(t) + V_j^-(t))$ with output impedance Z_m at each port is

$$V_i(t) = \sum_{j=1}^{N} \int_{-\infty}^{t} g_{ij}(t-\tau) E_j(\tau) d\tau = \sum_{j=1}^{N} g_{ij}(t) \star E_j \tag{4}$$

Here the symbol $\star$ denotes convolution, N is the number of external ports in the transmission line system and

$$g_{ij}(t) = \frac{1}{\Delta t} \mathbf{F}^{-1}[G_{ij}(\omega)] \tag{5}$$

is the time-domain Green's function or impulse response at port i and at time t to a Dirac delta source at port j and time zero, i.e. $g_{ij}(t) = V_i^-(t)/E_j(0)$. In (5)

$$G_{ij}(\omega) = \begin{cases} (1 + S_{ij}(\omega))/2 & i = j \\ S_{ij}(\omega)/2 & i \neq j \end{cases} \tag{6}$$

is the frequency-domain Green's function from port j to port i at radian frequency ω and $\mathbf{F}^{-1}[\,]$ is the inverse Fourier transform. Finally, Δt is the time increment of $g_{ij}(t)$ and is one half of the inverse of the highest frequency component (f_{max}) of the frequency-domain Green's function, i.e. $\Delta t = 0.5/f_{max}$, and T is the time span of the Green's function and is equal to the inverse of the frequency increment, Δf, of the S parameters $(T = 1/\Delta f)$.

3.1.1 Removing the Effect of the Reference Impedance

Following the approach in [6]. the effect of the reference impedance is removed by inserting a series impedance $-Z_m$ at each termination so that a virtual short circuit is created between the load and the transmission network as shown in Figure 10. This circuit can then be partitioned into a set of termination networks and one linear transmission line network as shown in Figure 11 where V_j is the node voltage at port j and V_j' is referred to as the virtual voltage at port j. These are related by

$$V_j'(t) = V_j(t) + I_j(t) Z_m \qquad j = 1, N \tag{7}$$

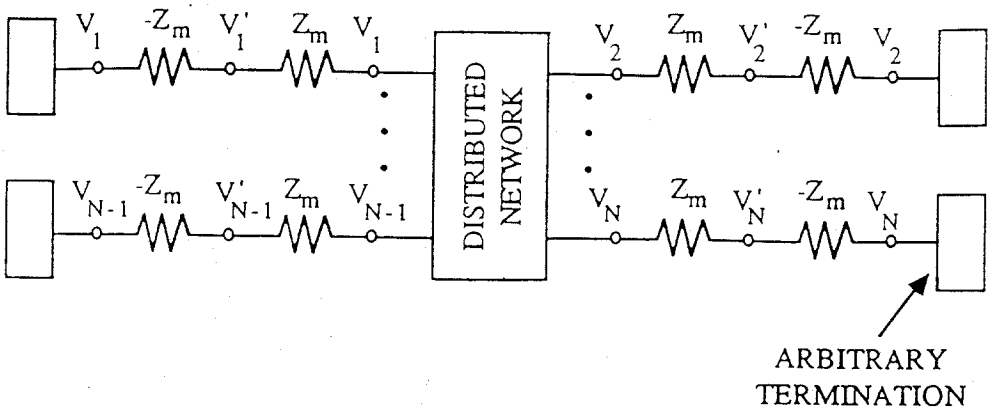


Figure 10: N port distributed system with reference impedances removed and arbitrary nonlinear terminations.

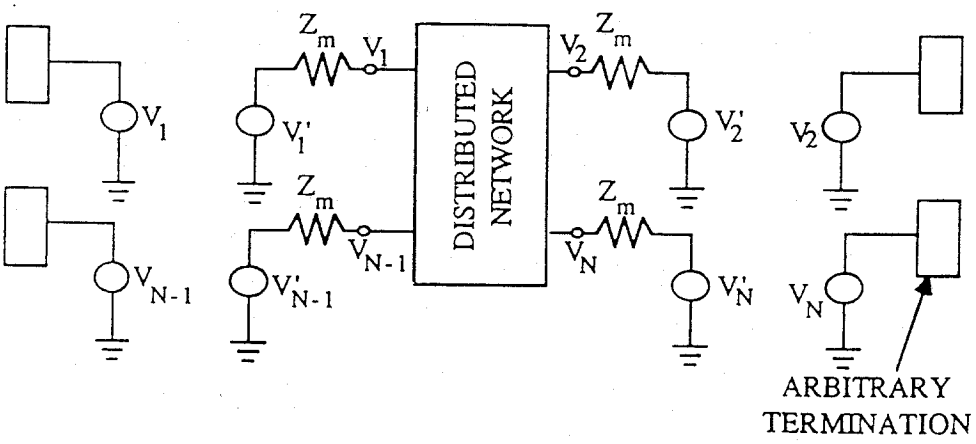


Figure 11: Distributed network partitioned into termination networks and a transmission line network.

where I_j is the current flowing into the distributed network at port j, or equivalently, the current flowing out of the arbitrary termination at port j and so, in general, is a nonlinear function of V_j. In discrete form (4) becomes

$$V_j'(n_t) = V_j(n_t) + I_j(n_t)Z_m \qquad j = 1, N \tag{8}$$

3.1.2 Development of Convolution Equation to Describe Transmission Line System

Applying the Green's function of (5) to the modified network of Figure 11 and using circular convolution leads to the convolution equation

$$V_i(t) = \sum_{j=1}^{N} g_{ij} \star V_j' = \sum_{j=1}^{N} \int_{-\infty}^{t} g_{ij}(t-\tau)V_j'(\tau)d\tau \tag{9}$$

which has the discrete form

$$V_i(n_t) = \sum_{j=1}^{N} \left[\sum_{n_\tau = 0}^{n_t} g_{ij}(n_t - n_\tau)V_j'(n_\tau) + \sum_{n_\tau = n_t + 1}^{N_T} g_{ij}(n_\tau)V_j'(0) \right] \tag{10}$$

In (10) N_T is the number of time points in the period of interest, $t = \Delta t.n_t$, and $\tau = \Delta\tau.n_\tau$. The introduced node sources V_i are now memory devices controlled by the present and past value of all virtual sources, the V_j''s, according to (10).

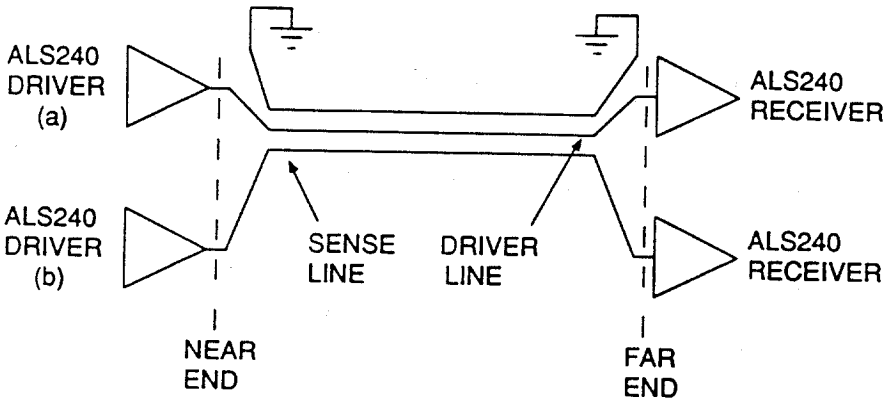


Figure 12: Complex transmission line test structure.

While being efficient, circular convolution does have restrictions as it requires that all transients in the system die out within the time span of the Green's function. This is not a great concern as the Green's function can be zero padded to ensure that all transients have died out within the extended functions time span. Practically it means that the time span of the maximum transient in the transmission line system must be estimated in advance.

3.2 Implementation in a Circuit Simulator

The above algorithm for transmission line network analysis can be quickly implemented in a transient circuit simulator with user defined nonlinear controlled voltage source elements and with subcircuits or macros. The user defined voltage sources implement discretized forms of (8) and (10). Our implementation of the transmission line model treats the node voltage source V_i as a nonlinear voltage source with the virtual sources, the V_i''s, being the controlling variables as in (10). Each virtual source, V_j', in turn is defined by (8). The circuit simulator calls this user defined routine once for each port and each iteration and performs the necessary nonlinear iteration to match the node voltage $V_i(n_t)$ given by (10) to the node voltage $V_j(n_t)$ used in (8) for all $i = j$.

Transient analysis of any circuit using a circuit simulator is accomplished in three distinct steps: setup, establishment of DC initial conditions, and transient analysis. During setup the transmission line model obtains the time domain Green's function from frequency-domain S parameters (supplied by the user or calculated by the simulator) which characterizes the transmission line network.

During DC initialization the transmission line network model performs a circular convolution using the Green's function (10) to return a steady state value for the voltages at each port based on the voltage and current at all ports. Finally during transient analysis the convolution using the Green's function is evaluated to find the present voltage at each port. In general, interpolation of the virtual sources is required as the simulation time step does not correspond to the discretized Green's function time step.

3.3 Results and Discussion

Verification of the transmission line model and its implementation was undertaken for the transmission line system of Figure 12. The transient response predicted by our model is compared with experimental results in Figures 13–16.

The digital devices were modeled at the transistor level and the transmission line network was experimentally characterized using an automatic network analyzer. The frequency increment was such that the time span of the derived Green's function was four round trip reflections. Evaluation of the Green's function took a small proportion of the total simulation time. Driver (a) was clocked at approximately 20 MHz and the input of driver (b) set its output to logic 0. Experimental measurements are difficult to make in coupled transmission line networks as the probe used in the measurement alter the reflection and crosstalk characteristics of a network. Nevertheless reasonably good agreement is obtained between the measured and simulated responses.

Panda, the placement tool will be discussed next.

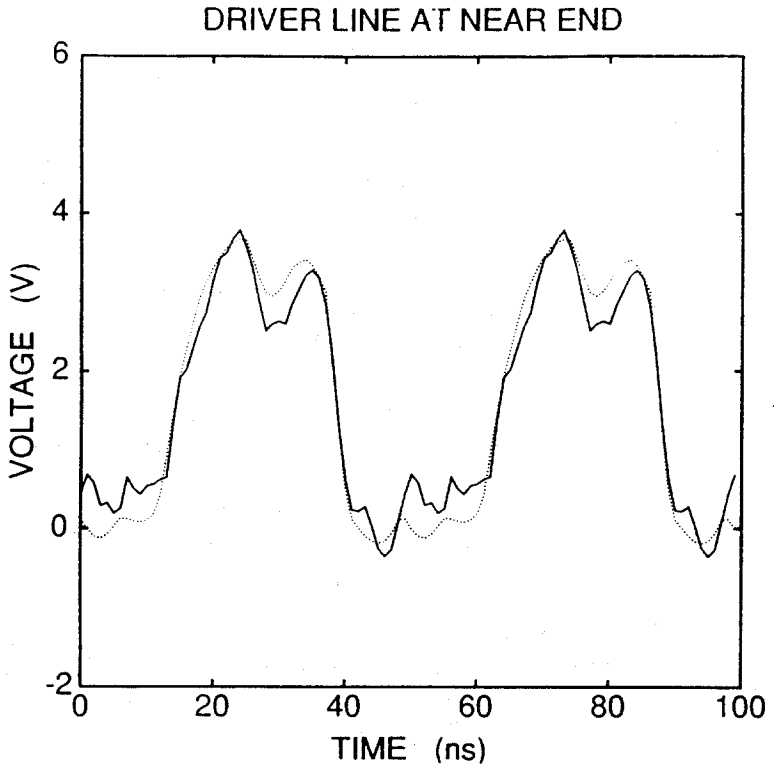


Figure 13: Measured (dotted curve) and simulated (solid curve) time-domain responses at the near end of the driver line.

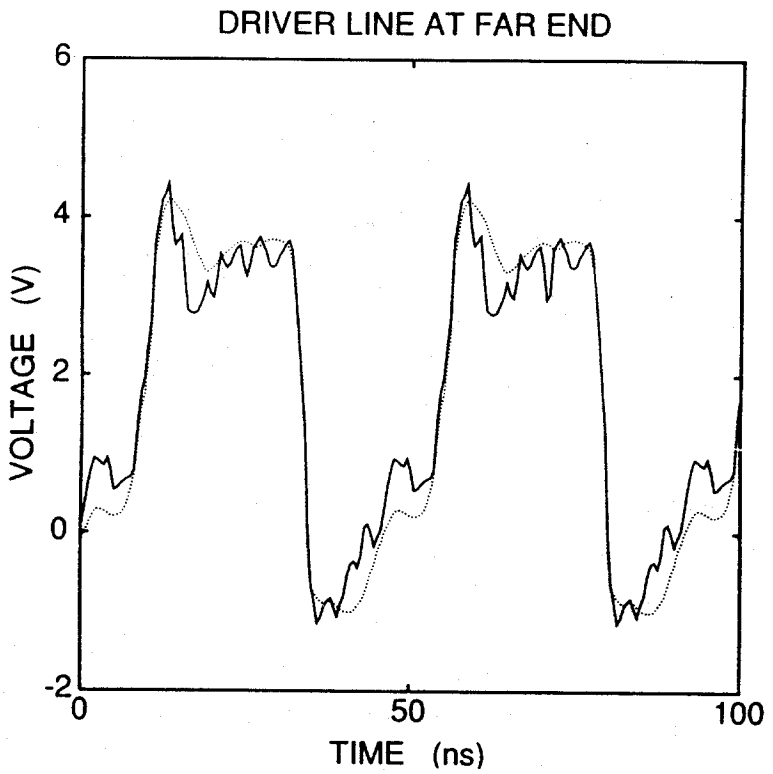


Figure 14: Measured (dotted curve) and simulated (solid curve) time-domain responses at the far end of the driver line.

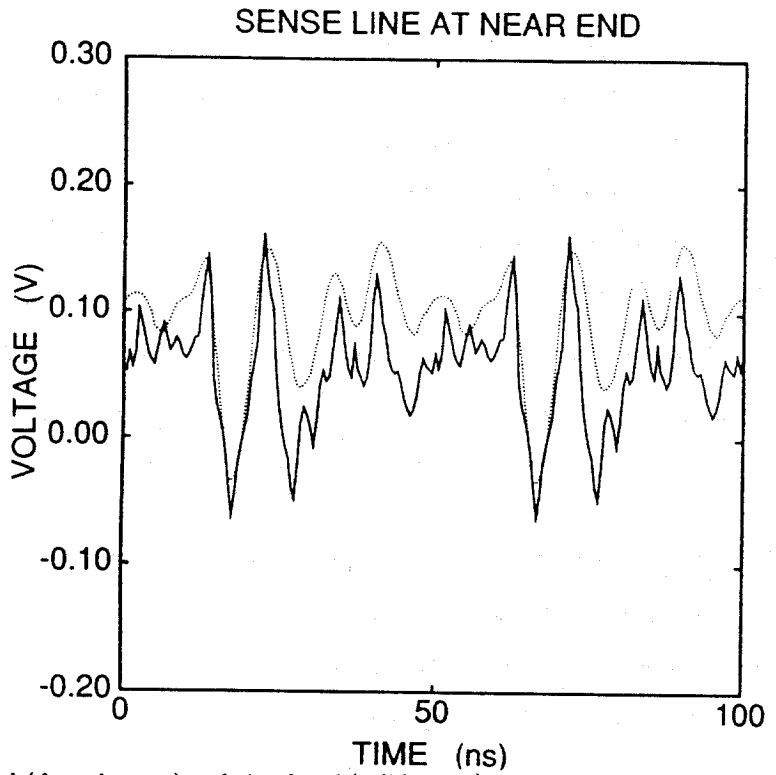


Figure 15: Measured (dotted curve) and simulated (solid curve) time-domain responses at the near end of the sense line.

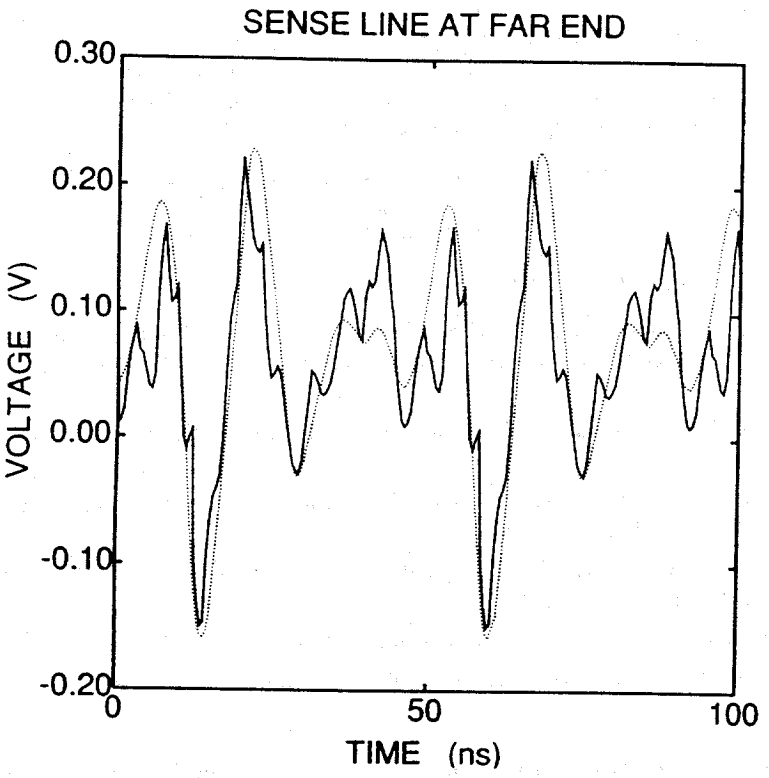


Figure 16: Measured (dotted curve) and simulated (solid curve) time-domain responses at the far end of the sense line.

4 Panda: Placement Tool Assistant

The placement of ICs on a multichip module is carried out with the following criteria in mind:

1. The placement must have a high probability of being routable by the follow-on routing tool.
2. The nets must be routable while meeting the timing requirements.
3. The ICs are placed so that thermal requirements are met.
4. An output is produced suitable for passing to the router.

It is assumed that the third criterion can be met by integration with an appropriate thermal analysis tool. This will not be addressed further here.

The placement assistant tool has three inputs: A components list, including pin-outs; a netlist specification; and a model base.

The netlist specification and the model base will be described before indicating how these are incorporated into the tool.

4.1 Netlist Specification Format

An example of the netlist specification is shown in Table 1. The netlist_specification is divided into two parts: connectivity and delay specifications.

The connectivity specification includes the following features:

1. Net connectivity. The pin identity for each terminal in the net.
2. Net type (clock, signal, bus, power, etc.) The purpose of this classification is to identify particular routing constraints in advance.
3. Net name. The first member of the group list specifies the global name of the net.
4. Net group(s). Nets are grouped based on logical requirements (eg. elements of a common data bus), timing requirements (eg. nets that must be routed together for timing reasons), and display and manipulation requirements (eg. groups of nets selected as being critical with regard to placement decisions.) Nets can be cross-listed between groups and grouped hierarchically for flexibility.

The delay specification allows for the following timing information to be entered:

1. The minimum and maximum delay allowed between each pair of pins.
2. Special timing or routing information, such as:
   (a) *Edge* indicating edge sensitive data. The timing field thus refers to minimum and maximum 50% delay for arrival of this edge. Before and after this arrival, noise and ringing must be controlled to prevent false switching.
   (b) *Level* indicating level sensitive data. The data must be stable for the specified period of minimum to maximum delay.
   (c) *Together_with* <*Group*> indicates that all signals belonging to group <*Group*> must arrive together at their terminals, within a certain time range.
   (d) *Relative_with* <*Net*> indicates that the timing specifications for this net are relative to the signal arrival times on another net, instead of absolute.
   (e) *Daisy Chain* will cause the net to be routed as a daisy chain with the pins in the order indicated.
   (f) *Steiner Tree* will cause the net to be routed as a minimum length Steiner tree.
   (g) etc.

Most of the timing information is provided for use by the routing tool. For multi-pin nets it is possible to indicate timing information for each pair of inputs and outputs.

$$ [A_1 A_2 AD_24 AD_25 ADD_26 ADD_27] BUS CONTROL_BUS mem_bus1 sys_interface_5

Table 1: Sample netlist specification for the placement tool.

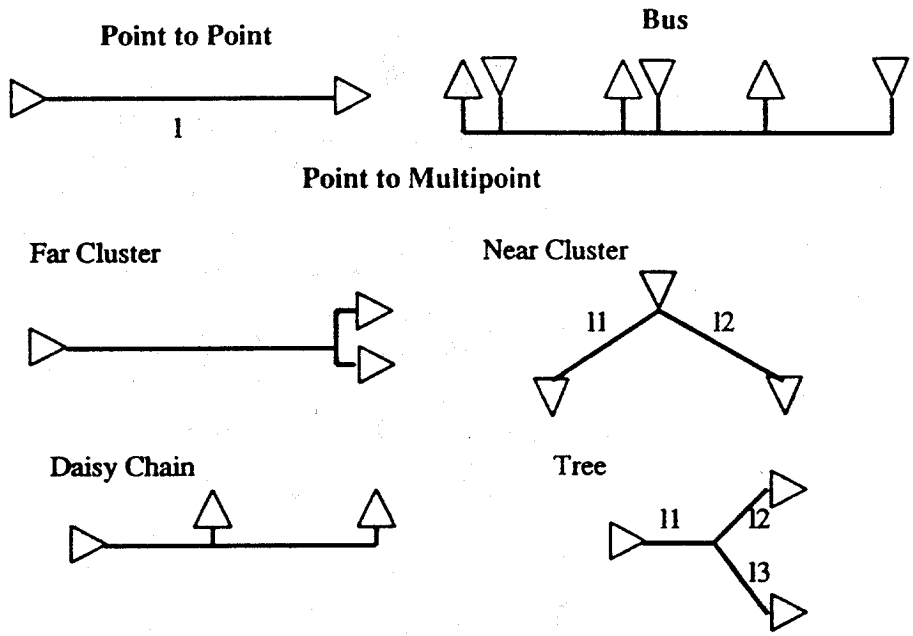


Figure 17: Types of Nets connecting drivers and receivers.

4.2 Model Base

The model base is the interface between the technology and the placement tool. It contains information regarding the average wiring density for the technology and simple models relating delay to placement. The equations used for the models are hard-wired into the tool. The data for the models is provided in a technology file. The models vary with the net type (see Figure 17). The models were developed by taking standard results in the literature (for example see [11], [5] [2], [1], [7]) and fitting them to a matrix of simulation-based experiments. For placement purposes the models do not have to be extremely accurate. These models have a better than 10% accuracy when compared with the simulation data.

The models for point-to-point and daisy-chain connections will be discussed first. The far-end cluster net type can be treated in the same manner as the point-to-point net type except that the load at the end of the line is larger.

4.3 Delay Models for Point-to-Point and Daisy-Chain Connections

The electrical model for a point-to-point connection is shown in Figure 18. Simulation results show that the effect of the discrete inductances in Figure 18 are negligible in the frequency range of interest. Thus a suitable equivalent circuit can omit these, as shown in Figure 19. Some sample transmission line simulations using this are shown in Figures 20 to 21.

Two factors contribute to delay in this model:

- The time-of-flight delay

$$l/v_{ph}, \tag{11}$$

where l is the length of the transmission line, and $v_{ph} = c/\sqrt{\epsilon_{eff}}$ is the phase velocity in the line (c is the speed of light in a vacuum and ϵ_{eff} is the effective dieletric constant of the line.)

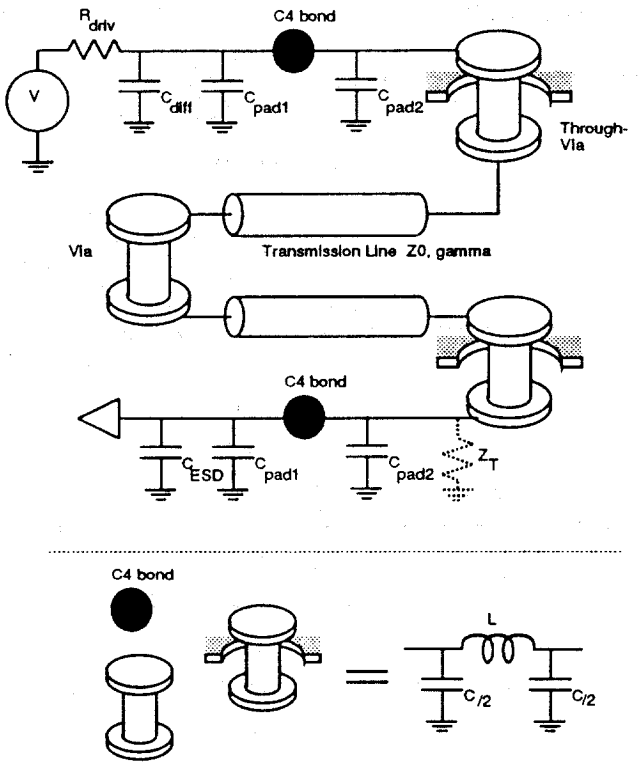


Figure 18: Full Electrical Model for a point to point connection in a multichip module. In the full model all parameters vary with frequency.

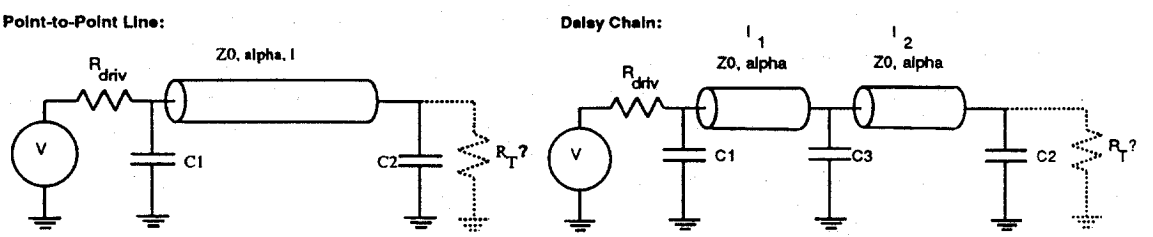
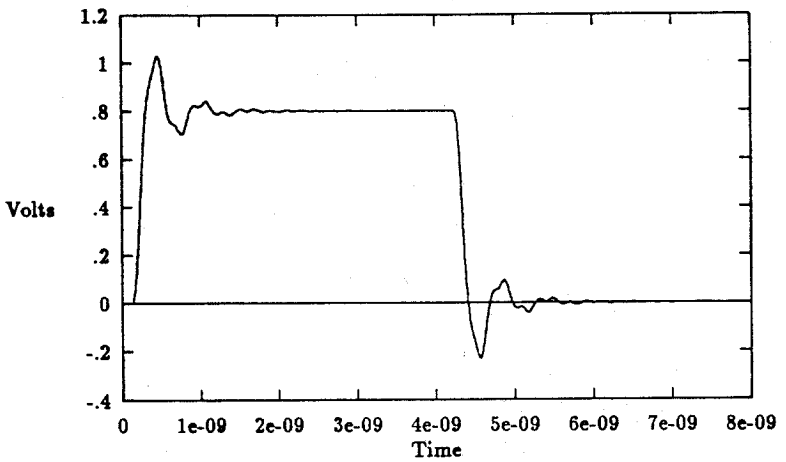


Figure 19: Simple electrical models suitable for calculating delay for a placement tool. Parameters are assumed to be fixed with frequency.



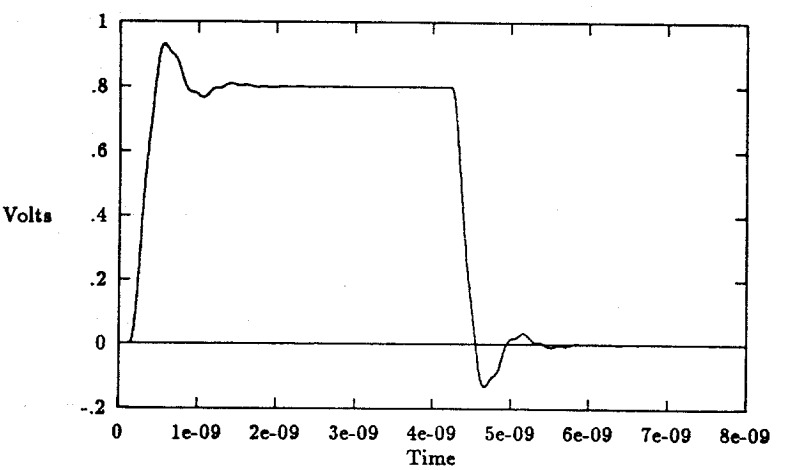
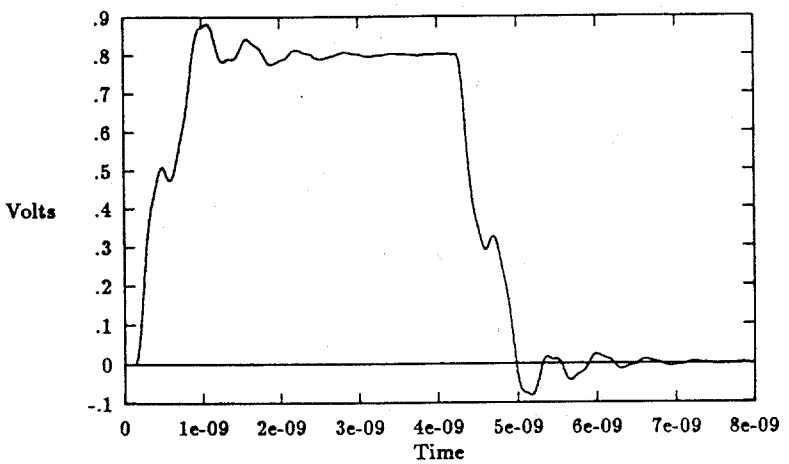


Figure 20: Simulation of a point-to-point line with $C1 = 2pF$, $R_{driv} = 25\Omega$, $Z_0 = 50\Omega$, no matching termination, and $R = 373\Omega/m$. The first simulation is for $C_2 = 1pF$, the second is for $C_2 = 3pF$.



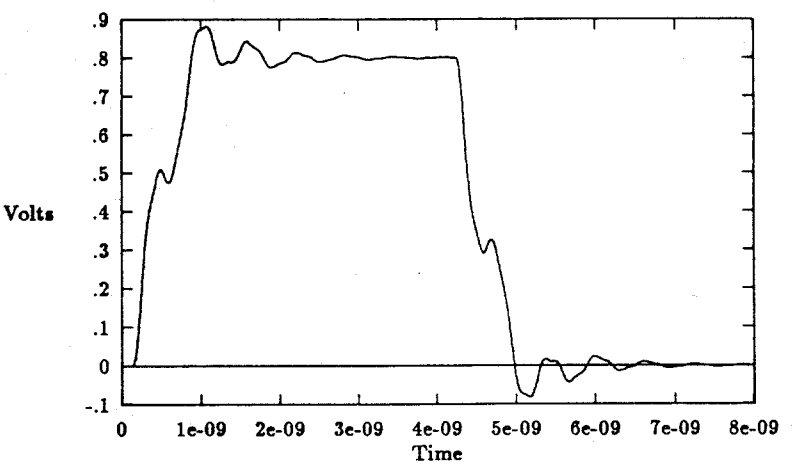


Figure 21: Simulation results for a daisy-chain line with $C1 = 2pF$, $C_2 = 3pF$, $C_3 = 3pF$, $R_{driv} = 25\Omega$, $Z_0 = 50\Omega$, no matching termination, and $R = 373\Omega/m$. The first simulation is for the mid-point terminal, the second for the end terminal.

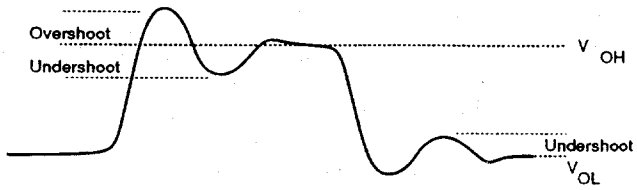


Figure 22: A ringing waveform.

- The capacitor charging delay. The rise time is degraded by capacitor charging. A reasonable value for this (50%) charging delay is

$$0.7Z_pC \tag{12}$$

where C is the value of the capacitance and Z_p is the equivalent charging resistance (for the daisy-chain structure in Figure 19, $Z_{p1} = Z_{driv} \parallel Z_0$; for capacitor C1, $Z_{p3} = 0.5Z_0$; for capacitor C3, and $Z_{p2} = R_T \parallel Z_0$ for C2. R_T is present if the line is matched at the termination to prevent reflections ($R_T = Z_0$,) R_T will not be present otherwise.)

The delay for a point-to-point line is

$$T_{point-to-point} = l/v_{ph} + 0.7Z_{p2}C2 \tag{13}$$

The delay to the end of a two-terminal daisy-chained line is

$$T_{end-chain} = \frac{l_1 + l_2}{v_{ph}} + 0.7Z_{p1}C1 + 0.7Z_{p3}C3 + 0.7Z_{p2}C2 \tag{14}$$

The delay to the center terminal of the two terminal daisy-chain is

$$T_{mid-chain} = (l_1/v_{ph}) + 0.7Z_{p1}C1 + 0.7Z_{p3}C3 \qquad \text{if } R_T = Z_0 \tag{15}$$

$$T_{mid-chain} = \frac{l_1 + l_2}{v_{ph}} + 0.7Z_{p1}C1 + 0.7Z_{p3}C3 + 0.7Z_{p2}C2 + 0.7Z_{p3}C3 \tag{16}$$

$$\text{if } R_T \text{ is not present (open circuit)} \tag{17}$$

$$\tag{18}$$

The requirement for a terminating resistance, R_T, is determined by the need to control ringing. As the presence or non-presence of R_T affects the delay, the placement tool will have to make a preliminary decision as to whether one is required or not. A ringing waveform is shown in Figure 22. Up to 35% overshoot and 10% undershoot is acceptable in ECL circuits [11]. Similar levels would apply to CMOS circuits. Often overshoot is controlled through the use of clamping diodes at the receiver. This will not be assumed here. Ringing is caused by reflections from the loads being reflected again at the receiver.

Consider the daisy-chain structure in Figure 19. The magnitude of the voltage wave placed on the line as a result of a transition at the driver is

$$V_{Start} = \frac{Z_0}{Z_0 + R_{driv}} V_{driv} \tag{19}$$

This voltage wave is attenuated at a rate of $e^{-\alpha l}$ as it travels down the line, where $\alpha = R/(2Z_0)$. Part of this wave is reflected back to the driver from the load capacitance at the mid-point terminal, and part of this wave may also be reflected from the end-point load. The pulse reflected from the mid-line terminal is re-reflected from the driver (unless the driver is matched with $R_{driv} = Z_0$) and eventually arrives at the end-terminal as a positive voltage with a magnitude of

$$V_{pulse} = |V_{Start} e^{-\alpha(3l_1+l_2)} \Gamma_{driv} \frac{C_3 Z_0}{2t_r}| \tag{20}$$

where

$$\Gamma_{driv} = \frac{R_{driv} - Z_0}{R_{driv} + Z_0} \tag{21}$$

is the amount reflected back from the driver, and t_r is the rise time of the signal [12]. This pulse may contribute to the overshoot, depending on its relative timing.

After charging C3, the main voltage wave travels down the line. At the end of the line part of the wave is reflected. This reflected component also acts to increase the voltage at the end of the line. There is little reflection if $R_T = Z_0$. In this case, the voltage at the end of the line is given by

$$V_{end} = V_{Start} e^{-\alpha(l_1+l_2)} \tag{22}$$

Losses (α) may cause this voltage to be insufficient to switch the receiving circuit. If the connection is not delay critical this is not a problem as the voltage at the end of the line will eventually reach V_{drive} [8]. If the line is delay sensitive, a matching termination can not be used, and ringing must be controlled through other means.

If there is no matching resistor, initially the capacitor C2 acts as a short circuit, producing a negative reflection. As the capacitor charges up, it acts like an open circuit, producing a positive reflection. The voltage at the end of the line is the sum of the incident voltage and the peak reflected voltage:

$$V_{end} = V_{Start} e^{-\alpha(l_1+l_2)}(1 + \Gamma_C) \tag{23}$$

where $\Gamma_C \leq 1$ is dependent on the value of C2 and the rise time t_r. V_{end} must be greater than the switching threshold voltage of the receiver and less than the acceptable peak overshoot.

With no matching termination, part of the incident wave is reflected from the receiver, and is reflected again from the driver to eventually arrive back at the receiver as an undershoot wave, with a magnitude of:

$$V_{under} = V_{Start} e^{-\alpha(3l_1+3l_2)} \Gamma_C \Gamma_{driv} \tag{24}$$

If the voltage at this time, ($V_{end} - V_{under}$), is less than the acceptable peak undershoot, then the ringing is excessive.

If a matching termination can not be used to control ringing, then these expressions for voltages at the end of the line indicate that ringing can also be controlled by manipulating R_{drive} (ie. adding series resistance to the driver) and α (ie. using different line geometries) [4].

Ringing is also not a problem if the total line delay, $T_{end-line}$, is some fraction of the rise time. Simulation studies show that ringing is not a problem if $t_r > (2 \text{ to } 3) \times T_{end-line}$, the exact ratio depending on the magnitude of the reflections. As the rise time increases further, the waveforms at the receivers will become a lot more uniform. The expressions for delay will however remain the same.

All of the effects can be seen in the sample simulation results given in Figures 20 and 21. Note that the mid-point receiver in a daisy-chain goes through a meta-state while waiting for the reflection from the end of the line. This may be a problem in an edge-sensitive net.

4.4 Delay Models for Near-End Cluster and Bus

The expressions for delay in a bus driven from one end take the same form as the expressions for delay in a daisy-chain. The delays for a near-end cluster and a bus driven from a mid-point can also be treated in a very similar fashion to a point-to-point and daisy-chain respectively, except that the voltage placed on the line initially is reduced to

$$V_{start} = \frac{Z_0/n}{Z_0/n + R_{driv}} V_{driv} \tag{25}$$

where $n = 2$ for a bus, and n is the number of loads for a near-end cluster.

4.5 Delay Models for a Tree Net

If a stub on a tree-net is electrically short,

$$t_r > (5 l_{stub}/v_{ph} + 0.7 Z_0 C_L), \tag{26}$$

then the stub can be treated as a lumped load with a capacitance equal to the sum of the load capacitance at the end of the stub and line capacitance.

If the stub is electrically long, then excessive ringing may result from the stub. This situation requires further analysis.

4.6 Panda: Design Overview

PANDA is built on top of the *VEM* graphical interface and fits into the *OCT* CAD Framework. Building PANDA into a framework allows easy and flexible integration with the other tool components. Eventually the simulator, Transim will interface with other tools through the same framework. In operation, the placement process is as follows:

- The user provides three files to the tool: Netlist_specification, Circuits_description, and Delay_specifications. The tool reads the circuits description and displays the blocks in *VEM* one block at a time, giving the user the freedom of deciding on the initial placement.
- The Netlist_specification is then read using a separate package "*Net.*"
- Timing information is read and stored with each net.
- The user then manipulates the placement until timing specifications are met (or it is determined that the timing specifications are too tight) and a routing solution seems possible. The tool provides a number of features to assist in this process:
  - The user may choose to display all of the nets at once, or choose specific nets or groups of nets for display. With the possibility of a system containing over 10,000 nets, maximum flexibility is provided in terms of net display choices. Graphical and textual inputs are allowed. Nets can divided into hierarchies as an aid to this process.
  - All nets will be checked to see if they meet the timing specifications, by comparing this specification with the delay calculated assuming rectilinear wiring and the wiring models contained in the model base. If the specification is not met, the pins and nets will be highlighted.
  - A rich set of geometry-manipulation commands is provided. The user can move any block and its connections as a unit on the display. Connectivity maintenance is very important feature for this type of problem due to the high number of pins.
  - A variety of feedbacks is provided to the user. On the display, the user can examine the wiring usage of his layout along the horizontal and vertical axes and compare it with the wiring capacity. The total predicted wiring requirements are also displayed.

Possible future enhancements to Panda will be discussed before concluding the discussion.

4.7 Future Work

Two important enhancements to this tool would be to (1) provide automatic assistance of grouping, or abstraction, of nets so that a "representative rats-nest" could be displayed instead of a full rats-nest of connections, and (2) automatically select an initial placement by adapting a suitable VLSI algorithm.

Currently, the placement tool calculates length assuming rectilinear wiring. Future MCM routing tools may allow multi-angle wiring [3] [9]. As experience is gained with these tools, new wiring length estimation methods will have to be formed.

5 Conclusions

Designing a high frequency multichip module is a complex task. With frequency dependent transmission line parameters and complex systems of coupled lossy lines, new simulation approaches are required. A simulation tool is described that meets these requirements.

Multichip modules also provide a very high density interconnect. Designing 10,000 nets though simulation studies is a daunting and inefficient task. Instead physical design tools must be developed that understand the nature of high speed interconnect and can produce designs that can meet tight timing requirements. The first tool in such a physical design tool suite, the placement tool Panda, is described.

5.1 Acknowledgements

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