Table-Based Modeling of Delta–Sigma Modulators Using ZSIM

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Abstract—**In this paper ZSIM, a nonlinear *Z*-domain *SIM*ulator for sampled data systems, is presented and verified. ZSIM integrates analytic tools, a difference equation simulator, a novel table-based nonlinear *Z*-domain simulator, and digital signal processing into a workstation environment to provide fast and accurate simulation of delta-sigma modulators. The use of table-based simulation enables simulation of circuit nonidealities including clock feedthrough and saturation. Benchmark comparisons of difference equation simulations and table-based simulations are presented for delta–sigma modulators suitable for use in voice-band coders.**

I. Introduction

DELTA-SIGMA modulation [1] is one of a class of systems which use oversampling and 1-bit quantization to achieve high-resolution A/D conversion at a lower rate. Oversampling is attractive in that precise analog antialias filtering can be omitted. Instead digital finite-impulse response (FIR) low-pass filters, which are relatively insensitive to coefficient roundoff, are used after the modulator to perform decimation and anti-alias filtering. Decimation is required to achieve conventional pulsecode modulated signals by reducing the sampling rate of the 1-bit data stream generated by the modulator. Delta–sigma modulators can be implemented with few precision circuits and precise component tolerances are not needed [2], [3]. They can be implemented in digital MOS IC technologies through the use of switched-capacitor circuits [4], [5]. Delta–sigma modulators have been successfully used in voice-band CODECS [3] and for the U-interface of an integrated services digital network (ISDN) where monolithic high-resolution A/D conversion is required for echo cancellation [4].

The circuit topology of a first-order delta–sigma modulator is that of a nonlinear, sampled-data, closed-loop control system used as a signal tracking device shown in Fig. 1. The system has as its input an analog signal, $x(t)$, which is encoded as a digital pulse stream, $p(t)$. The feedback minimizes the error signal

$$e(t) = \int [x(t) - p(t)]\, dt \qquad (1)$$

which is quantized, sampled, and then held for one clock cycle by a comparator. The output, $p(t)$, is, therefore, driven to match $x(t)$ in an integrated error sense. Sample waveforms for the delta–sigma modulator are shown in Fig. 2.

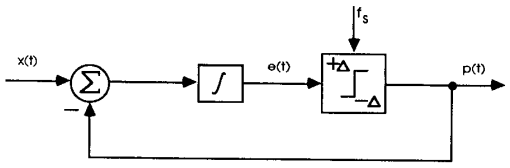

Fig. 1. Block diagram of a first-order delta–sigma modulator.

Although delta–sigma modulation is conceptually simple, the system is difficult to analyze. The nature of the modulator's structure prohibits simple analysis—the feedback loop introduces stability problems, it contains a mix of continuous analog and sampled digital signals, and includes nonlinearities. Consequently the implementation and widespread use of delta–sigma modulators is partly limited by the inadequacy of analytic and simulation tools. Recent developments in analytic techniques for delta-sigma modulators [6]–[12] have increased the understanding of signal-to-distortion performance, quantization noise spectra, and stability of these circuits. However, only numerical simulations can provide the required confidence in design, final optimization of system performance, and verification of novel circuit topologies. Until now, numerical simulation of components of delta–sigma modulators have been restricted to time-consuming circuit-level simulators (e.g., SPICE [13]), and numerically efficient difference equation simulators which simulate complete systems but which cannot capture many circuit phenomena [14]. The speed of simulation is of overwhelming importance as the circuit must be simulated for a large number of clock cycles, often tens of thousands, to obtain signal-to-noise or signal-to-distortion information. The main goal of this work was to develop a simulator for delta–sigma modulators which could capture the effects

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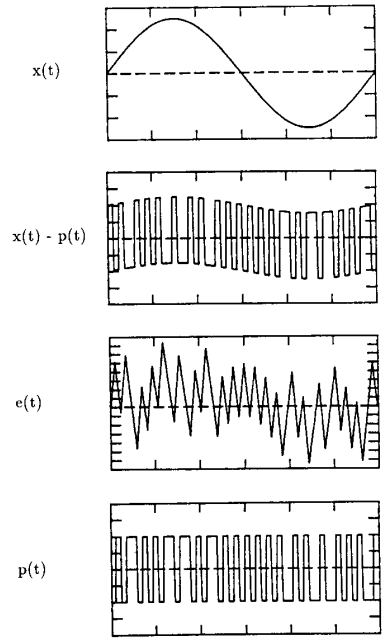

Fig. 2. Sample set of signals for a first-order delta–sigma modulator.

of circuit nonidealities such as incomplete settling, clock feedthrough, and amplifier saturation in a fast and efficient manner. These are both in agreement with analytic results we have obtained [12].

We present a new simulator called ZSIM (nonlinear z-domain *SIM*ulator) which provides fast and accurate simulation of nonlinear sampled-data systems. The purpose of this work is to obtain simulation throughput with little sacrifice in simulation results. Speed and accuracy are achieved by using tables to characterize subcircuits. These tables are obtained via circuit-level simulation using an external routine similar to SPICE. Table look-up methods have been used recently in the speedup of computer-aided analysis in the areas of MOSFET modeling [15]–[18] and distributed microwave circuits [19]. Here we apply ZSIM to the simulation and computer-aided design (CAD) and analysis of delta–sigma modulators. ZSIM represents an extension of the conventional difference equation simulation technique as multidimensional table look-up replaces difference equation evaluation. ZSIM is the last component of a CAD tool for delta–sigma modulator design currently under development at North Carolina State University. The system integrates analytic tools [8], [12], a difference equation simulator, and a table look-up simulator, and includes decimation, baseband filtering, and post-processing (see Fig. 3).

In the following sections, the development of ZSIM is discussed with benchmark comparisons of table-based simulations and difference equation simulations. Computational speed comparison of the table-based simulator versus conventional circuit-level simulators are presented.

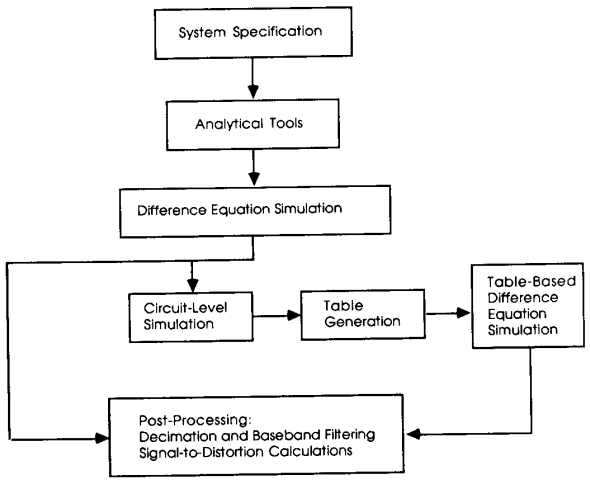

Fig. 3. Flowchart of a CAD tool for delta–sigma modulators.

II. Development and Structure of ZSIM

Delta–sigma modulators can be treated as sampled-data systems, so it is possible to model the performance of individual subcircuits of a modulator at the sampling intervals. Continuous-time information, such as the circuit waveform between sampling intervals and the circuit state at internal subcircuit nodes, are not required for accurate system-level simulation. Thus it is possible to use a discrete-time or z-domain description of the system. The utility of difference equation simulators is that they operate with linear (z-domain) equations and so computations are kept to a minimum. Often, however, it is not possible to develop sufficiently accurate difference equations because of complex dependencies on nonlinearity, clock feedthrough, slew-rate limiting, and finite gain-bandwidth product of subcircuits. ZSIM, using table methods, is a natural extension of difference equation simulation and enables these effects to be modeled using a multidimensional table.

The development of ZSIM is analogous to that of the difference equation method. A second-order delta–sigma modulator is shown in Fig. 4 and, with the insertion of fictitious sample-and-holds before each integrator, can be represented in the z-domain as shown in Fig. 5 together with digital anti-alias filtering and decimation. In most delta–sigma implementations there is only one clock cycle delay and in the block diagram we have incorporated this delay in the second integrator. This representation enables the subcircuits to be considered individually (although the input and output loading of the subcircuits must remain unchanged as the tables are developed). Since practical monolithic implementations of delta–sigma modulators are sampled-data circuits and/or switched capacitor circuits, the addition of the fictitious sample-and-holds, if placed appropriately, has no effect on circuit performance.

Consider the first integrator block of Fig. 5. The output of this block can be modeled by a linear difference equa-

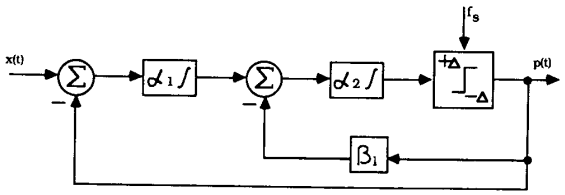

Fig. 4. Block diagram of a second-order delta-sigma modulator.

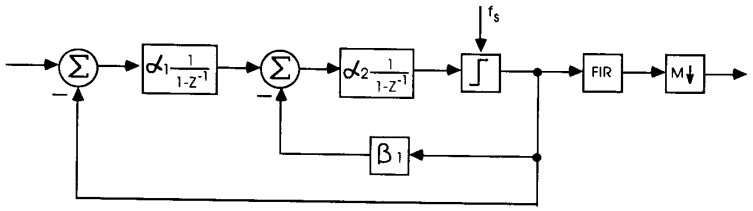

Fig. 5. Second-order z-domain delta-sigma modulator with FIR anti-alias filter and decimator.

tion:

$$y[k] = y[k-1] + \alpha_1(x[k] - p[k]) \qquad (2)$$

where $y[k]$ is the integrator output, $p[k]$ is the comparator result held over from the previous cycle, and k is the sample index. The limitation of this function is that it is linear, although saturation can at least be partially modeled by limiting the output $y[k]$ to maximum and minimum values. Physical circuits may contain gain errors, saturation, and clock feedthrough effects which have no linear relationship to their inputs. More generally, $x[k]$, $y[k-1]$, and $p[k]$ are independent variables for $y[k]$ with an unknown nonlinear relationship:

$$y[k] = T(x[k], y[k-1], p[k]) \qquad (3)$$

where T, as implemented in ZSIM, is a table look-up function.

A. Program Structure

ZSIM is a modular program consisting of four major subdivisions—an input module, a table generator module, a simulator module, and a post-processor module. ZSIM is written in ANSI standard Fortran 77 and has a user-friendly input format. The input module's high level input capability allows for input to be taken from the keyboard and/or from a disk file. Standard English commands are used to diminish the need for a specific program environment language.

The table generator module develops the tables that describe the input–output characteristics of each subsystem. This involves running a circuit-level simulator for one clock cycle, automatically extracting pertinent data, and repeating the process until each position of the table contains simulated data. This process is not fully integrated into the ZSIM environment.

The simulator module performs simulations of the sampled-data circuit using table descriptions of individual subsystems or using difference equations for rapid circuit investigations. The order of simulation for each subsystem at each clock cycle is as follows: the input signal generator, the integrators in the order of signal propagation, and the comparator. The voltages at the input and output nodes of each subsystem are stored in memory for processing during the next clock cycle.

The post-processor module implements decimation and baseband filtering and calculates system performance characteristics. Filtering of the modulator output is included here since in most applications the oversampled data must be decimated to a usable frequency. Both FIR decimating filters and IIR baseband filters can be specified. Fast Fourier transform (FFT) and other signal analyses are available to determine the signal-to-noise ratio (SNR) and signal-to-distortion ratio (SDR) of the complete system or of any of the data sequences. Thus an FFT may be calculated for the modulator bit stream or the decimated and filtered output. Initial data points, which represent transient circuit performance, can be ignored. The SDR is calculated as the ratio of the total spectral power (less both dc and signal powers) to the signal power. Noise is treated as a distortion component so that SDR is the ratio of noise plus harmonic distortion to fundamental signal power. As the sinusoidal input signal may not correspond to a single FFT bin several bins around the signal bin are combined to determine the actual signal power with appropriate corrections to the white noise calculation. Similarly, several bins are used to determine the dc level in the presence of aliasing. The SNR is evaluated the same way except that harmonic distortion components are not included.

B. Tables

The representation of circuit subsystems by tables allows discretization of input/output data in both linear and nonlinear regions of operation. A block diagram of an in-

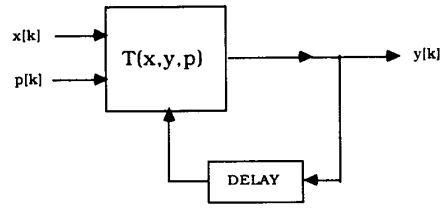

Fig. 6. A ZSIM integrator block.

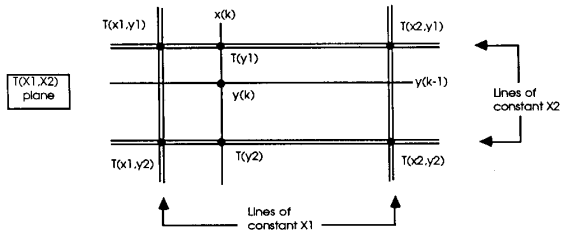

Fig. 7. A planar view of table grid with interpolation points.

tegrator modeled in ZSIM is shown in Fig. 6 and described by (3) where the output of the integrator, denoted $T(x, y, p)$, depends on three variables: the input signal $x[k]$ at the kth clock cycle, the integrator output $y[k-1]$ at the previous cycle, and the current comparator output $p[k]$ which is sampled and held from the end of the previous cycle. Therefore, $p[k]$ is a discrete (binary) variable while $x[k]$ is a continuous variable that can range between the power supply rails, and $y[k-1]$ is a continuous variable that is limited by the operational amplifier saturation levels. Thus if N discrete values are selected for $x[k]$ and M discrete values are selected for $y[k-1]$, a $2 \times N \times M$ table will describe the operation of the integrator. The table is essentially divided into 2 two-dimensional tables, each representing one of the two possible discrete values for $p[k]$.

C. Interpolation

Linear table interpolation is used in ZSIM and is considered to be adequate for delta-sigma modulators where the system components should be designed to be approximately linear. Linear interpolation retains monotonicity and continuity but introduces discontinuities in the derivatives of the table function. Higher order interpolation methods are currently being implemented and may be necessary for applications with stronger nonlinearities.

Since the comparator output value is binary, no interpolation is needed between the $T(x, y, -1)$ and $T(x, y, +1)$ planes. Therefore, in each subtable, an integrator output becomes a function of two variables, $T(x, y)$, defining a plane (see Fig. 7). Generally, the input values and the previous output values will not coincide with the discrete graph points, so interpolation is necessary. Interpolation proceeds as follows: four $y[k]$'s are selected from the table: $T(x_1, y_1)$, $T(x_2, y_1)$, $T(x_1, y_2)$, $T(x_2, y_2)$. Using the actual $x[k]$ value, linear interpolation between $T(x_1, y_1)$ and $T(x_2, y_1)$ produces $T(y_1)$, and interpolation between $T(x_1, y_2)$ and $T(x_2, y_2)$ yields $T(y_2)$. Then linear interpolation of $T(y_1)$ and $T(y_2)$ given $y[k-1]$ yields the desired approximation of $y[k]$. A small error will occur in the nonlinear regions of the integrator due to the use of linear interpolation. It is possible that with improved interpolation routines a more accurate model of the linear and nonlinear regions could be obtained with fewer table points.

III. Simulation of a Voice-Band Delta-Sigma Modulator

The following results demonstrate the use of ZSIM to validate the design of a voice-band delta-sigma modulator. Two examples are used. In the first design, nonidealities are suppressed through careful circuit design and through the use of a low sampling frequency (1.024 MHz), thus enabling direct comparison of difference equation and table-based simulations. The second design differs from the first in that the MOSFET switches have been increased fivefold in both length and width. This produces significant errors as a result of charge feedthrough of the clocking waveforms. The effect of these switching errors on overall modulator performance can be determined using ZSIM with table representations of the switched capacitor integrators. Tables have been constructed using both SPICE and CAzM (circuit analyzer with macromodeling) [18] for each integrator of the delta-sigma modulator. Comparison of results obtained using both sets of tables demonstrates the importance of using a charge-based circuit simulator.

The topology of the modulator and decimator circuit is as shown in Fig. 5 and $\alpha_1 = 0.1$, $\alpha_2 = 0.5$, and $\beta_1 = 0.1$. The selection of β_1 insures that the range of voltages at both inputs of the second integrator are roughly equal. The sampling frequency is 1.024 MHz, which is low enough that finite slew-rate and finite bandwidth effects are insignificant. Furthermore, the integrators do not go into saturation or exhibit significant clock feedthrough effects (in the nominal case), so the results of the table-based simulation should be comparable to the difference equation simulation results. The FIR decimation filter has parabolic weighting with 128 taps to provide the necessary out of band noise rejection [8], [20]. The sampling rate is first reduced by a factor of $M = 32$ to obtain a data stream at 32 kHz. Then an IIR digital filter is used to limit the signal bandwidth to 3.4 kHz. Finally, the sampling rate is further reduced by a factor of 4 to obtain an 8-kHz data stream. An FFT is performed on this signal to evaluate SNR and SDR.

For the benchmark study, 40 960 clock cycles were simulated, and the first 8192 points were discarded to obtain a 32 768 point data record. After decimation, 256 samples were available for SNR and SDR anaysis using a 256 point FFT. An input signal frequency of 406.25 Hz was selected for the simulations reported here. This frequency corresponds exactly to the 14th bin of the FFT, so that little spreading or leakage of the signal fundamental across the baseband spectrum occurs. At the same time,

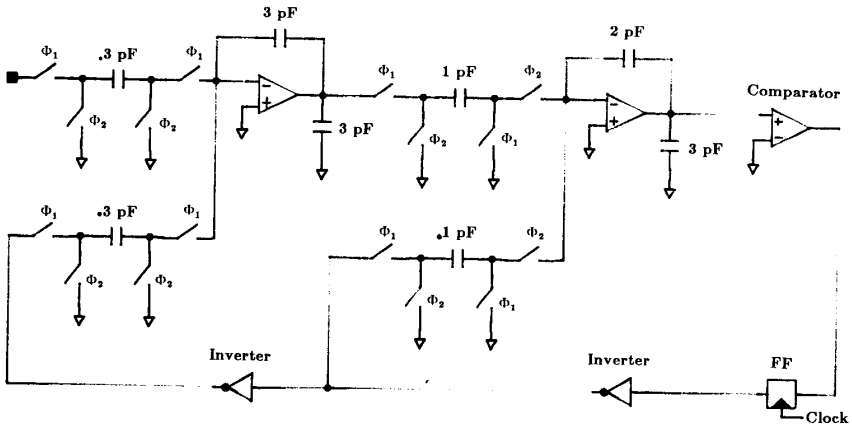

Fig. 8. Second-order delta-sigma switched-capacitor circuit.

this frequency is incommensurate with the sampling frequency, so that distortion components of the signal do not all lie on submultiples of the system clock. However, if an off-bin signal frequency is used, elaborate windowing with, for example, the Blackman–Harris or Kaiser–Bessel windows [26], must be used to minimize signal spreading and leakage. With only 256 points, the spreading of the signal and its harmonics occupies most of the baseband spectrum and so even with an appropriate window, it is practically impossible to discern the true noise floor of the modulator. However, with a very large number of samples (obtained at the cost of large computation times and increased memory usage) it should be possible to obtain meaningful SNR measures for off-bin signals. Although both Hamming and Blackman–Harris windows are available in ZSIM, best results are obtained when the signal is on the bin. For off-bin signal frequencies, the signal power (or the power at a signal harmonic) is computed in a neighborhood around the main peak, with a correction for the surrounding noise floor. This neighborhood is then excluded from the noise plus distortion calculation, and again a correction is made for the noise which has been removed.

The switched-capacitor implementation of the delta-sigma modulator is shown in Fig. 8, and the operational amplifier is shown in Fig. 9. The topology for each switched-capacitor integrator ensures that its transfer function is independent of parasitic capacitances between any node and ground [21], [22]. The class AB operational amplifier was designed using a 1.25-μm CMOS process supported by the Microelectronics Center of North Carolina. The operational amplifier operates from a single 5-V power supply, so that the input and the comparator output swing ± 2.5 V relative to analog ground (2.5 V). Φ_1 and Φ_2 are nonoverlapping clocks, each with a duty cycle close to 50 percent. The first integrator's output is stable at the end of Φ_1 and the output of the second integrator is valid at the end of Φ_2. Note that the clock timing causes the first integrator to have negative gain and the second integrator to have positive gain. The negative gain of the first integrator is corrected by the additional inverter in the feedback path, and the modulator will actually encode $-x(t)$.

A. Table Generation

A dc analysis of the class AB operational amplifier was used to determine the upper and lower saturation limits of $+1.25$ V and -1.45 V relative to analog ground. Difference equation simulations were used to determine the range over which table values would be required. For the first integrator the analog input ranges from -2.5 to 2.5 V with respect to analog ground, while the output ranges between ± 0.65 V. Therefore, the discretization points for the table were chosen to be $x[k] = -2.5$, -1.75, -1.0, -0.5, -0.1, 0.1, 0.5, 1.0, 1.75, 2.5, and $y[k-1] = -0.7$, -0.5, -0.3, -0.1, 0.1, 0.3, 0.5, 0.7. The input to the second integrator clearly ranges from -0.65 to 0.65 V, and the output ranges between -1.5 and 1.5 V. For the second table, we chose $x[k] = -0.7$, -0.5, -0.3, -0.1, 0.1, 0.3, 0.5, 0.7, and $y[k-1] = -1.5$, -1.3, -0.8, -0.4, -0.1, 0.1, 0.4, 0.8, 1.3, 1.5. As a table entry 0 V was avoided to prevent spurious distortion figures for small signals due to slight asymmetries around it which could arise from numerical errors in the circuit simulators. The number of discretization points was chosen to obtain a reasonable computation time. Each table required approximately 2 h to generate running CAzM on a Convex C1 (equivalent to about 12 h on a 1 MIP workstation).

One set of tables was generated using SPICE version 2.G6 and a second set was generated using CAzM. In both cases the LEVEL2 MOSFET model was used. However, SPICE2.G6 uses a capacitance-based formulation of this model while CAzM is strictly charge based. A series of individual transient circuit simulations were performed to build up the tables one point at a time. Some precautions must be considered during these simulations. First, the integrator output and other signal path nodes must be correctly initalized for each run. Second, the timing of the switched-capacitor integrator during table simulation must

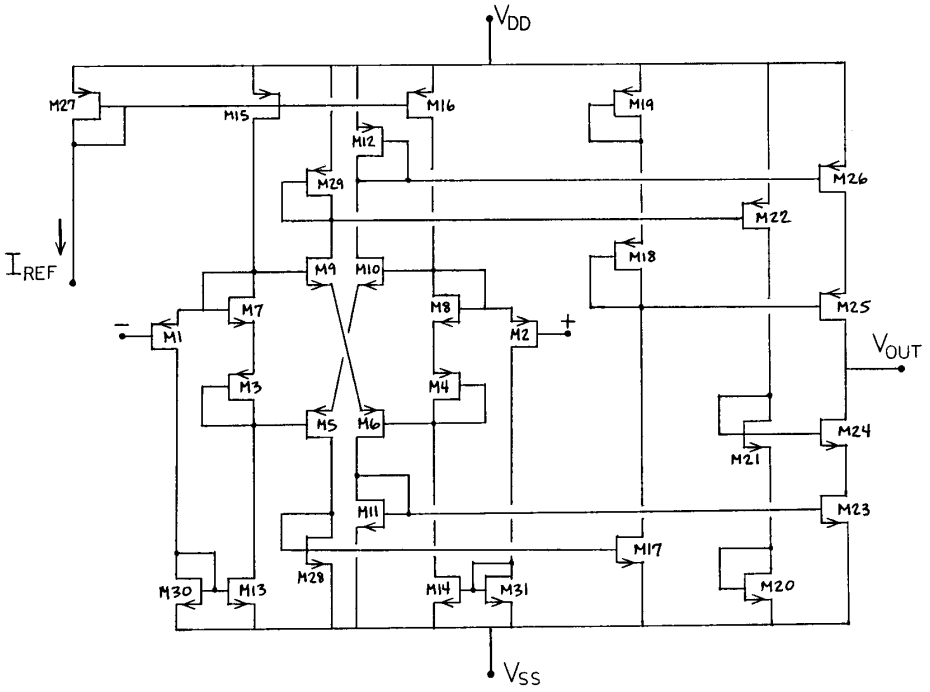

Fig. 9. Class AB operational amplifier.

match the timing of the complete modulator. In particular, the critical time points for each node must be correctly identified. Here, each simulation began 10 ns before the end of the prior clock cycle and continued for precisely one clock period, ensuring that node initialization occurred during the correct phase of the clock. (Many nodes in the circuit will not be initialized correctly if the simulation runs begin between clock phases.) The integrator nodes were initialized by forcing an initial condition on the feedback capacitor. Forcing the integrator output to a desired value with a voltage source does not produce correct initialization unless the virtual ground node is simultaneously initialized to the correct offset voltage of the amplifier. In contrast, forcing the initial voltage across the capacitor correctly initializes both the output and virtual ground nodes.

Both the CAzM table values and the SPICE table values differ from the ideal difference equations for the switched-capacitor integrators. Part of these errors reflect the simple offset and gain errors of the switched-capacitor integrators. Offsets arise from charge feedthrough, primarily from the switch at the virtual ground node. Linear gain errors arise from the finite gain of the operational amplifiers. Offset and gain errors have only a minor effect on the overall modulator performance, and in particular do not contribute to harmonic distortion. The remaining error components must come from actual circuit nonlinearities or from errors in the transient circuit simulations used to construct the tables. Nonlinearities in the circuit can arise from actual nonlinearity of the operational amplifier transfer curves or from signal dependencies in the charge feedthrough components. For the SPICE tables, large errors are present which are not found in the CAzM results. In particular, the table points obtained using CAzM vary at most 4 mV from the ideal curves (for the nominal design) while the SPICE table points vary as much as 20 mV from the ideal curves. Moreover, the errors in the SPICE tables are less smooth than in the CAzM tables. As an example, Fig. 10 shows the errors (difference from the ideal difference equation) for one row of the first integrator tables using both SPICE and CAzM. It is well known that capacitance-based circuit simulation of nonlinear dynamic circuits is inaccurate due to nonconservation of charge arising from numerical integration errors. This phenomena has been demonstrated in SPICE by several authors [23], [24]. Similar discrepancies have been observed by us between SPICE and SCAMPER, a proprietary circuit simulator developed by Bell Northern Research. These results appear to establish that charge conservation is critically important for accurate table generation, and that the use of some versions of SPICE should be avoided.

B. Simulation Results

Simulations were performed for the nominal voice-band circuit using ideal difference equations, SPICE tables, and CAzM tables. Calculated SDR (signal to distortion plus noise) curves are shown in Fig. 11 for each case with an input range of -60–-2 dB relative to a full scale (5-V peak-to-peak) sinusoid. Accurate and repeatable SDR

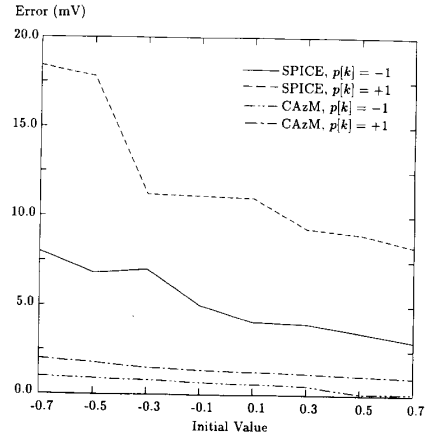

Fig. 10. Comparison of SPICE and CAzM table data. The initial value is $y[k-1]$ and the error is the difference between the ideal $y[k]$ and that simulated.

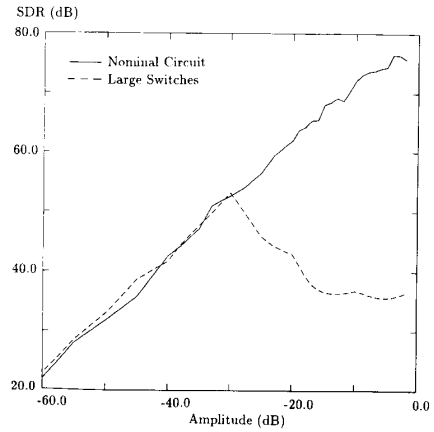

Fig. 12. SDR versus input amplitude for the nominal circuit and with oversized switches.

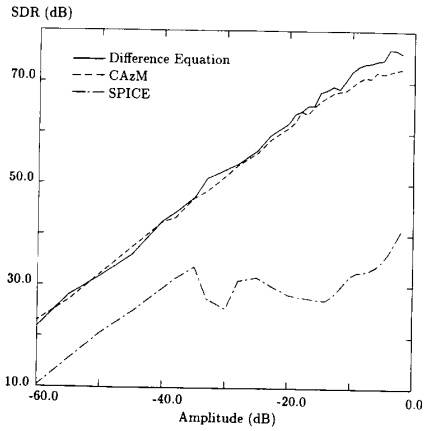

Fig. 11. SDR versus input amplitude using ideal difference equations, CAzM tables, and SPICE tables.

calculations require simulation for 2^{15} clock cycles yielding 512 baseband FFT bins after decimation. An additional 512 points are simulated and discarded to allow the initial circuit transient to disappear. The CAzM and ideal difference equation results are in close agreement whereas the SPICE results are clearly erroneous.

A second set of CAzM tables was generated using the same circuit as in Figs. 8 and 9 except with MOSFET switches that were enlarged by five times in both length and width. The large switches magnify the charge feedthrough effect, producing an input referred offset of more than 80 mV. Since the charge feedthrough is weakly dependent upon the resistance of the input switches, it is also somewhat signal dependent. This signal dependence introduces harmonic distortion in the overall modulator. The ZSIM SDR calculations using the large switch CAzM tables is plotted in Fig. 12 along with the results for the nominal circuit. For small signal levels, the SDR calculation is dominated by noise and the two curves are nearly identical. As the signal level increases, the distortion components grow faster than the signal level so that the SDR drops off dramatically. The distortion components for the large switch case thus limit the maximum achievable SDR performance. Although the switching errors have been highly exaggerated, this example demonstrates how the table based method employed in ZSIM can be used to validate a circuit design. Tables constructed as described above will capture clock feedthrough errors, and errors arising from finite amplifier gain or nonlinearity. Errors arising due to finite slew rate or finite bandwidth (incomplete settling) are only partially captured since the table point simulations assume that the switched capacitor integrators start from steady state at each clock cycle. Since the integrator tables depend only upon the current inputs and the previous output, they cannot be used to simulate supply injection or capacitor hysteresis. These effects could be captured using tables with higher dimensionality, however, the CPU time required to construct the tables would become prohibitive.

C. Table Validation

While the example above illustrates the use of ZSIM as a design tool, it does not provide a true validation of the use of tables to capture the behavior of a complete delta-sigma circuit. Although significant distortion components were observed using tables for the case of the large switches, it would be impossible to confirm these results by calculating the SDR performance directly using CAzM. As discussed in the next section, such a simulation would require more than 10 years of CPU time. Therefore, a second investigation was performed of a simpler, first-order delta-sigma modulator similar to that of Fig. 8 and again using the operational amplifier of Fig. 9 and with oversize switches. In this case, CAzM was used to perform a 40-cycle simulation of the complete modulator with a large sinusoid as an input. The output of the switched capacitor integrator was recorded at the end of each clock cycle, and this sampled waveform was compared to the

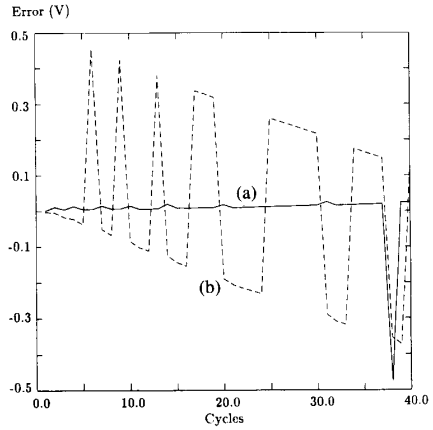

Fig. 13. Errors in integrator waveforms in a delta-sigma modulator simulation using ZSIM with CAzM tables, curve (a), and ZSIM with ideal difference equations, curve (b), relative to that in a direct CAzM simulation.

first 40 cycles of a ZSIM simulation using the tables generated with CAzM. In order to have a significant change in the input over the 40 cycles a 4-V peak-to-peak input waveform was used. Ideally, one would expect the ZSIM table-based results to match the direct CAzM simulation. The difference between the two waveforms is plotted as the solid curve in Fig. 13. The comparator decisions match through the 37th cycle, at which point the integrator outputs differ by 19 mV. For comparison, the dashed curve shows the difference between an ideal difference equation simulation and the direct CAzM simulation. In this case, the comparator decisions disagree after only 5 cycles, and the integrator outputs differ by 370 mV after 39 cycles. Clearly the table-based simulation provides a much more accurate representation of the complete modulator than the difference equation. The error in the table-based simulation accumulates at a rate of roughly 0.5 mV per cycle, which is a small fraction (less than 5 percent) of the per cycle charge feedthrough, and we have found that it corresponds to a ceiling on the SDR calculations of about 80 dB [25].

The conclusion that can be drawn from these results is that since the table-based simulation matches the full transient simulation for so many cycles, our assumption that the internal states of the delta-sigma modulator can be ignored is good. There is only a very small residual effect, presumably due to incomplete settling of internal nodes, that is not captured. However, by increasing the dimensionality of the table to include the external states two cycles earlier, as well as the states at the previous cycle, residual effects could be modeled. So, while starting to become unwieldly, the general method of table-based simulation presented here can be extended to higher precision circuits.

D. Computational Speed

ZSIM table-based simulation takes 3 min and the FFT/SDR calculation takes 2 min for a total of 5 min on a 1 MIP microvax II. Therefore, a complete (35 point) SDR versus amplitude curve, as in Fig. 11, takes 3 h. In addition table generation would take the equivalent of 12 h on a 1 MIP computer. In contrast, if CAzM were used alone, 35 runs of 40 960 cycles per run would be required at approximately 4 min per cycle for a total of 95 000 h. Clearly it is impractical to evaluate the system level performance of a delta-sigma modulator using a transient simulator alone. By capturing the circuit behavior in tables, the simulation problem is reduced to a manageable size.

IV. Conclusions

A new fast and accurate CAD tool for delta-sigma modulators has been described. The program incorporates analytical tools, difference equation simulation, and circuit-level simulation through the use of a novel table-based nonlinear z-domain simulator (ZSIM). The tool includes various post-processing functions such as decimation, baseband filtering, and signal-to-distortion ratio calculations. The approach has been validated by comparing difference equation and table-based simulations for a voice-band coder both with and without circuit nonidealities.

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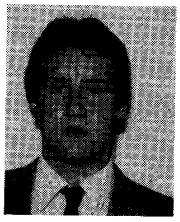

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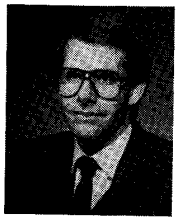

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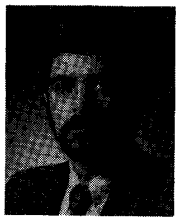

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