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Table-Based Simulation of Delta-Sigma Modulators

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***Abstract*—The program ZSIM (nonlinear *Z*-domain SIMulator) is used to explore the benefits and limitations of a table-based approach to the simulation of delta–sigma modulators with switched-capacitor integrators. Simulations demonstrating the effects of clock feedthrough and incomplete settling are presented, as well as simulations demonstrating the importance of the use of an accurate and charge conservative circuit simulator for the table point transient simulations. The methods used are appropriate for other discrete time systems where simulation of system-level performance is desired based on the results of transient circuit simulation.**

I. INTRODUCTION

Delta–sigma modulators [1] are one of a class of A/D converters that use oversampling to achieve a high level of precision at a lower sampling rate. Delta–sigma modulators can be implemented with few precision circuits and the component tolerances need not be precise [2], [3]. Also, delta–sigma modulators are easily implemented in digital MOS IC technologies through the use of switched capacitor integrators [4], [5].

A block diagram of a first-order delta–sigma modulator is shown in Fig. 1. The analog input signal $x(t)$ is encoded into a digital pulse stream $p(t)$. The feedback loop minimizes the error signal $e(t)$, where

$$e(t) = \int [x(t) - p(t)]\, dt. \tag{1}$$

The error signal is quantized, sampled, and held for one clock cycle by the comparator to produce one output pulse. The system attempts to track the input signal $x(t)$ with the encoded output stream $p(t)$, so that the output $p(t)$ matches the input $x(t)$ in an integrated error sense. The pulsetrain $p(t)$ is a pulse density representation of $x(t)$, and the input can be reconstructed by passing the pulsetrain through a low-pass filter. In most applications, the pulsetrain is filtered and decimated to a lower sampling frequency to provide a more conventional PCM (pulse code modulation) representation of the input with high signal-to-noise ratio (SNR). The discrete time equivalent of Fig. 1 can be

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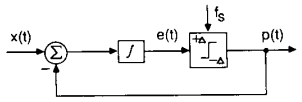

Fig. 1. Block diagram of a first-order delta–sigma modulator.

implemented using a switched-capacitor integrator. The error signal $e(t)$ is now represented by the following difference equation:

$$e[k] = e[k-1] + (x[k] - p[k]) \tag{2}$$

where $p[k]$ is the sampled and held result of the previous comparator decision.

Delta–sigma modulators are difficult to simulate since tens of thousands of clock cycles are required in order to obtain meaningful measures of SNR or signal-to-distortion ratios. Using accurate transistor-level circuit simulation, the transient analysis of a single clock cycle of the switched capacitor integrator may take several minutes of CPU time on a minicomputer or workstation. Detailed signal-to-noise curves would, therefore, take months or years of CPU time. Alternatively, difference equation models of the integrator can be used with dramatically reduced simulation time, but it is not easy to capture the actual nonidealities of the circuit in such a model. These nonidealities include the effects of finite bandwidth and slew rate of the operational amplifier, charge dump from the MOSFET switches, and nonlinearity of the amplifier transfer curve. Most of these effects can be modeled individually using difference equations. However, combinations of these effects are extremely difficult to model analytically, and the models obtained may only approximate the actual circuit behavior.

II. ZSIM

ZSIM (nonlinear *Z*-domain SIMulator) [6], [7] combines the speed of difference equation simulation with the completeness of a transistor-level simulator. ZSIM uses tables (one table for each integrator) which are generated by a transistor-level simulator. Each table is a discrete representation of the nonlinear difference equation for a switched capacitor integrator which includes the effects of actual circuit nonlinearities. ZSIM uses these externally generated tables to quickly simulate the modulator over several thousand clock cycles.

ZSIM can be used to simulate delta–sigma modulators using either ideal difference equations or externally generated tables. ZSIM includes FFT-based signal analysis routines to compute SNR, signal-to-total harmonic distortion ratios (STHD), and signal-to-(noise + THD) ratios (SDR), as well as baseband spectra. ZSIM also generates a histogram of the table usage which allows the user to determine the most efficient table discretization.

The tables used by ZSIM allow for the discretization of the input and output data for the linear and nonlinear regions of operation of the integrator. The output of an ideal integrator can be represented by

$$y[k] = y[k-1] + \alpha(x[k] - p[k]) \tag{3}$$

where $x[k]$ is the input signal during the current clock cycle, $y[k-1]$ is the integrator output from the previous clock cycle, $p[k]$ is the current output of the comparator which was sampled at the end of the previous clock cycle, and α is the integrator

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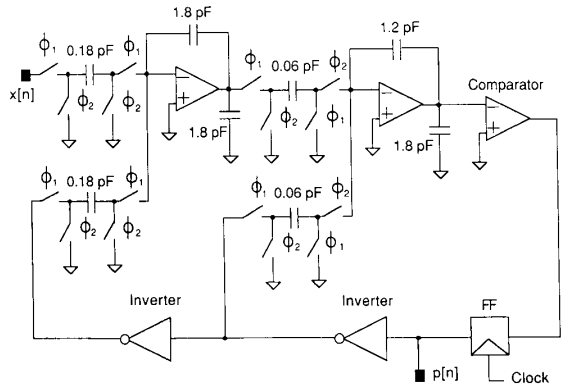

Fig. 2. Schematic of the second-order delta–sigma modulator.

gain. The output of the binary comparator, $p[k]$, is discrete, but the input signal $x[k]$ and the integrator output $y[k-1]$ are continuously valued and can, in general, range between the power supply rails. Therefore, the integrator tables are effectively divided into 2 two-dimensional tables (planes), with each plane corresponding to one value of $p[k]$. Within each plane, the rows represent the discretization of the input signal $x[k]$ and the columns represent the discretization of the previous integrator output $y[k-1]$. The table-based representation of the integrator can, therefore, be described by

$$y[k] = T(x[k], y[k-1], p[k]) \tag{4}$$

where $T(x, y, p)$ denotes an interpolation of the table data. In its current form, ZSIM uses linear interpolation. Linear interpolation is considered to be adequate for delta–sigma modulators since the system components are designed to be approximately linear. The goals of this paper are: 1) to explore the limitations in table-based simulation as a result of finite precision in the transistor-level transient analyses used to construct the integrator tables and 2) to explore the effects of circuit limitations in delta–sigma modulators such as incomplete settling and charge dump from the MOSFET switches.

III. Circuit Description

The circuit used in this study is a second-order delta–sigma modulator using switched capacitor integrators. The schematic for this circuit is shown in Fig. 2. The switches are composed of an n-channel MOSFET in parallel with a p-channel MOSFET in order to minimize clock feedthrough (charge dump) [8]. These switched-capacitor integrators require the use of a two phase clock. The inputs to the modulator must be valid before the rising edge of clock phase ϕ_1 and must remain valid for the duration of that clock phase. The output of the first integrator is valid at the end of clock phase ϕ_1, and the output of the second integrator is valid at the end of clock phase ϕ_2. Each clock has a rise/fall time of 4 ns. The clock phases are aligned such that there is a 2-ns delay between the falling edge of ϕ_1 and the rising edge of ϕ_2 and vice-versa.

The modulator is simulated for a 14-bit digital audio application, suitable for low-grade consumer electronics. For this application a clock rate of 5.6448 MHz is used with a decimation factor of 32, yielding a 176.4-kHz sampling frequency. In a typical application, this 4x oversampled data stream would be filtered and decimated again to obtain a 20-kHz signal bandwidth at a 44.1-kHz sampling rate.

The operational amplifier used to implement the switched capacitor integrators is a single-ended class AB amplifier operating from a single 5-V supply. The amplifier has an offset of 0.125 mV, a dc gain of 20000, and a unity-gain bandwidth of 20 MHz. The first (inverting) integrator has an input gain of 0.1 and a feedback gain of 0.1. The second (noninverting) integrator has an input gain of 0.5 and a feedback gain of 0.05. With these gains, typical simulations show an output swing of about -0.6 –0.6 V for the first integrator, and an output swing of about -0.8 –0.8 V for the second integrator with respect to analog ground (2.5 V). The table discretization of the columns (input values) of the first integrator table was chosen to be 0, -5, -10, -20, and -30 dB relative to a full scale swing of 5 V_{pp}. These levels correspond to ± 2.5, ± 1.4, ± 0.8, ± 0.25, and ± 0.08 V. The discretization of the rows (initial output values) of the first integrator table was chosen to accommodate the expected output swing of the integrator. The discretization points for $y[k-1]$ range from -0.9 to $+0.9$ V in increments of 0.2 V. The discretization of both the input (columns) and previous output (rows) for the second integrator table is identical to the discretization of the previous output of the first integrator. Discretization points at 0 V were avoided to prevent spurious distortion of small signals due to small slope discontinuities near zero.

IV. Generating Tables

In order for ZSIM to produce accurate results, the integrator tables used by ZSIM must be accurate. To accomplish this the transistor-level circuit simulator used must be capable of accurately simulating switched-capacitor integrators, the correct timing must be maintained during the table point transient analyses, and the table point transient analyses must start from the correct initial conditions. Tables were generated using both SPICE (version 2G.6) [9] and CAzM (Circuit Analyzer with Macromodeling) [10], [11]. In both cases the LEVEL 2 MOSFET model was used. CAzM is a table-based circuit simulator developed at the Microelectronics Center of North Carolina. CAzM has two advantages over SPICE. First, since CAzM is a table-based simulator, it is significantly faster than SPICE. Second, CAzM is a strictly charge-based simulator. Using SPICE, the switched-capacitor integrators operating at 5.6448 MHz exhibited errors of up to 20 mV relative to the ideal difference equations. Using CAzM, errors of less than 2 mV were observed. Fig. 3 shows the errors relative to the ideal difference equation for one row of a table using both SPICE and CAzM. Fig. 4 compares the SDR curves generated using both CAzM and SPICE tables to the SDR curve generated using ideal difference equations. These simulations were performed for a 2576.25-Hz input signal, and the noise calculations assume a 20-kHz bandwidth of interest. It is clear from Fig. 4 that the tables generated with CAzM predict more ideal performance than do the tables generated with SPICE. The greater accuracy seen in the CAzM tables is believed to be due to the fact that, unlike SPICE, CAzM is strictly charged-based and completely free from conservation of charge errors. In contrast, SPICE 2G.6 is capacitance-based, and it has been established that capacitance-based simulation is not accurate for nonlinear dynamic circuits since charge is lost as a result of numerical integration errors [12], [13]. It is especially important to keep track of charge in switched capacitor circuits, since small errors in charge can accumulate to produce an appreciable error over the transient analysis. Therefore, it is important to avoid the use of capacitance-based circuit simulators (such as SPICE) to generate the integrator tables.

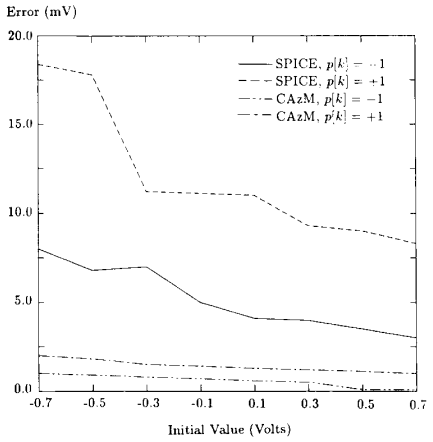

Fig. 3. Errors of SPICE and CAzM tables relative to ideal difference equations.

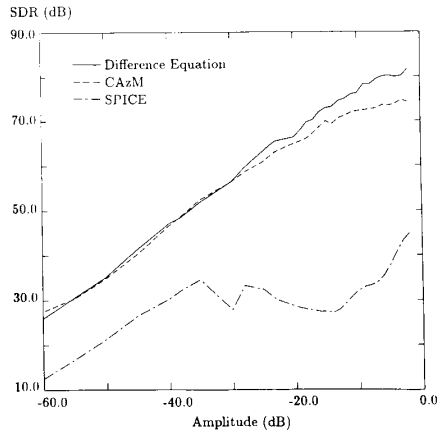

Fig. 4. SDR versus amplitude using 5.6448-MHz CAzM tables, SPICE tables, and ideal difference equations.

Another important consideration when generating integrator tables is the timing used during the transient analysis. This timing must exactly mimic the operation of the integrators during normal operation. The table point simulations must begin just prior to the end of the previous cycle and then continue for one clock period; it is critical that the simulations begin when the assumed initial condition is valid. Referring to Fig. 2, the simulation of the first integrator must begin just prior to the end of clock phase ϕ_1, and the simulation of the second integrator must begin just prior to the end of clock phase ϕ_2.

Finally, it is critical when generating integrator tables to ensure that the transient analysis starts from the correct initial conditions. Since the points in the table are determined by simulating the circuit for a given input value and a given initial output for the integrator, it is important that the output of the integrator not drift before the first clock change. As an example, the table for integrator #1 was created using the circuit configuration shown in Fig. 5. The inductor (1 MH) acts as a short circuit at dc, allowing the circuit to converge to the proper initial condition at the virtual ground node for the given initial output voltage. The voltage source V_s is varied from -0.9 to 0.9 V in increments of 0.2 V to create the $y[k-1]$ initial conditions. As the transient

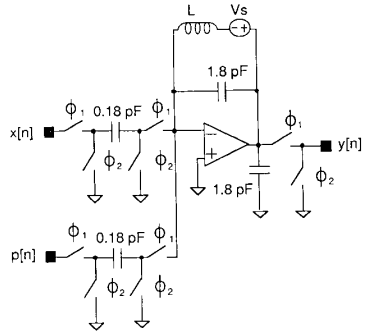

Fig. 5. Circuit configuration for table generation.

analysis begins, the inductor effectively becomes an open circuit which disconnects the voltage source. The switches at the output of the integrator are necessary to account for the loading effects of the second integrator. These switches also can produce errors in the first integrator due to ac coupling of the switching transients back through the feedback capacitor. Therefore, it is important to include these switches when generating the table for integrator #1. The circuit used to generate the table for integrator #2 was identical to Fig. 5 except that there were no switches at the output of the integrator.

V. Results of ZSIM Simulations

This section discusses the results of ZSIM simulations for three variations of the delta–sigma modulator and some of the problems associated with table-based simulation. The first configuration is the nominal case, where the modulator is clocked at 5.6448 MHz. This circuit is nearly ideal and performs at the limit of the accuracy of CAzM's transient analysis. The second case is the same circuit clocked at 11.2896 MHz. The higher clock rate is interesting since it can provide true 16-bit digital audio performance with a decimation factor of 64. However, to facilitate comparison to the 5.6448-MHz case the ZSIM simulations for this case are identical to the 5.6448-MHz case, except that 11.2896-MHz integrator tables are used. This case is used to examine the effects of finite bandwidth and slew rate of the operational amplifier and provides an example of spurious errors which may occur during transient analysis. In the third case, the widths and lengths of the switches are increased by a factor of five to examine the effects of charge dump from the MOSFET switches.

A. Nominal Case

In the nominal case the circuit is clocked at 5.6448 MHz, and the circuit errors are almost negligible. The SDR curve generated using CAzM tables tracks the SDR curve using ideal difference equations fairly well, as shown in Fig. 4, up to a signal level of -30 dB. In an actual design situation it would be critical to determine at this point whether the discrepancy above -30 dB is due to nonlinearity in the circuit or due to artifacts in the table generation process. Some indication can be obtained by examining the tables themselves.

The tables generated using CAzM (or SPICE) can be compared to tables generated using the ideal difference equations, and several error measures can be calculated. First, a table of point by point differences between each CAzM table and an ideal table was calculated. The average value of this difference table was then computed and removed, to eliminate the integrator

output-referred offset. The offset error is due to the offset of the op-amp and charge dump from the switches and does not greatly affect the SNR or SDR performance. The slopes of the rows of the difference table was then calculated. These values were averaged, and the linear error was subtracted from the offset corrected difference table. This eliminates the linear gain error of the integrator, which again does not significantly affect the SNR or SDR performance. This linear gain error arises due to the finite dc gain and finite bandwidth of the operational amplifier. Finally, an overall rms error was calculated using the adjusted difference table with offset and linear gain errors removed. This error represents only the nonlinearities of the circuit and/or random errors arising from the finite precision of the circuit simulator. Spurious or random noise in the tables will cause the entire SDR curve to shift downward, while actual saturating nonlinearities in the circuit will cause the SDR curve to flatten out or fall off at higher amplitudes.

Using this methodology, the offset errors for the CAzM tables for the nominal circuit were found to be -0.25 mV for integrator #1 and -0.44 mV for integrator #2. The linear errors were -0.035 mV/V and -0.141 mV/V for integrators #1 and #2, respectively. The remaining rms nonlinear error was 0.14 mV for table #1 and 0.15 mV for table #2. (In comparison, the corresponding rms nonlinear errors for the SPICE tables were 12.8 and 37.0 mV.) The 14-bit digital audio application has a dynamic range approaching 85 dB. This application requires the table precision to be on the order of 0.05 mV. Notice that the rms error of 0.1–0.2 mV is not sufficient to obtain the 85-dB SDR required for this application. The errors in the adjusted difference table appear to be primarily random in nature, which would seem to indicate a limitation in the table point simulations rather than the actual circuit. The tolerances used in the CAzM simulations were $chgtol = 10^{-16}$, $abstol = 10^{-11}$, and $reltol = 10^{-3}$. Tightening these tolerances provides little improvement in the simulation results and leads to prohibitively long simulations.

B. Increased Clock Rate

The simulations for the 11.2896-MHz case are identical to those for the 5.6448-MHz case except that the clock rate in the CAzM simulations was increased to 11.2896 MHz. By increasing the clock rate, it is possible to examine the effects of finite bandwidth and slew rate of the operational amplifier. The SDR curves for the 11.2896-MHz tables are shown in Fig. 6. While generating table #1 for this case, three spurious data points were obtained during transient analysis. These three errors occurred for an initial output value of -0.1 V and input values of -0.25, -0.08, and 0.08 V. A graphical representation of the spurious points is shown in Fig. 7. This figure shows the difference between the CAzM tables and ideal tables calculated from ideal difference equations. ZSIM simulations were performed both with the raw tables and with corrected tables where the three spurious points were replaced with linear interpolations of the surrounding points. The effect of these three spurious points can be seen in Fig. 6. The rms nonlinear error was 3.83 mV for table #1 and 11.88 mV for table #2. The rms nonlinear error for the corrected version of table #1 was 4.00 mV. Notice that although correcting the three spurious points in table #1 provides a dramatic improvement in SDR performance, it actually degrades the rms nonlinear error of the table. No conclusive explanation has been found for the spurious table points.

Another important issue raised by this case is the issue of incomplete settling. Errors can occur due to the fact that the integrator response is underdamped and the residual ringing is sampled at the end of the clock cycle. These oscillations may be responsible for the increased noise observed in the 11.2896-MHz case as indicated in Fig. 6 by a downward shift in the SDR curve. There is also more distortion than in the 5.6448-MHz case as reflected by the flattening out of the SDR curve at a lower SDR level.

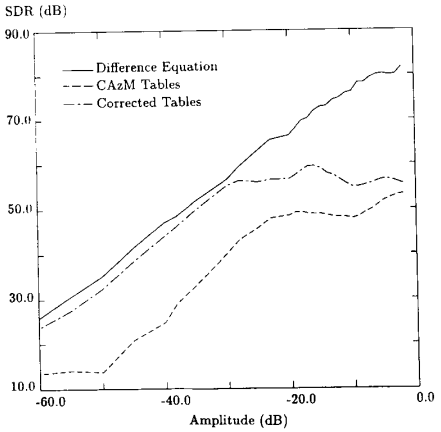

Fig. 6. SDR versus amplitude using 11.2896-MHz CAzM tables, corrected CAzM tables, and ideal difference equations.

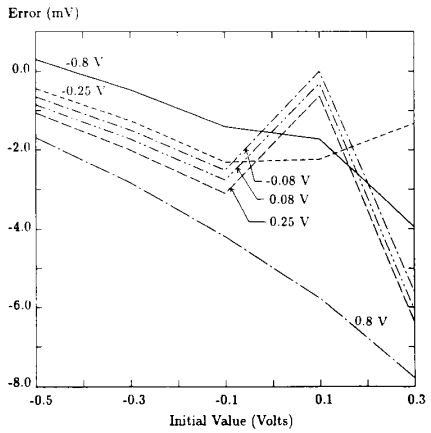

Fig. 7. Errors of CAzM table at 11.2896 MHz relative to ideal difference equation.

C. Enlarged Switches

A final simulation was performed in which the widths and lengths of the switches were increased by a factor of five. By increasing the size of the switches it is possible to examine the exaggerated effects of charge dump from the MOSFET switches. Charge dump (or clock feedthrough) is a common problem in switched capacitor circuits. When a MOSFET is turned off, the charge stored in the channel flows out of the source and drain of the device. A common practice to reduce this problem is to put a p-channel device in parallel with an n-channel device, so that the stored charges will cancel. This configuration requires separate clocks for the p-channel and the n-channel devices, which must be 180 degrees out of phase. While this technique reduces the charge dump, it does not completely eliminate it. The charge feedthrough produces an output referred offset in the switched-

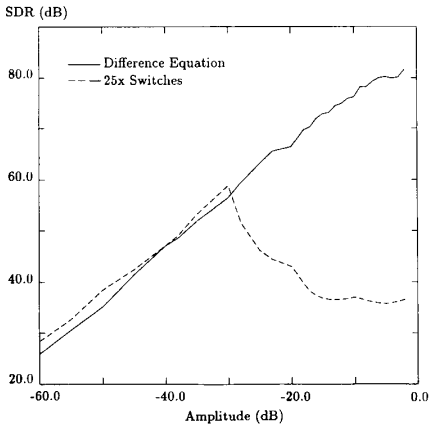

Fig. 8. SDR versus amplitude using 5.6448-MHz CAzM tables with 25x switches and ideal difference equations.

capacitor integrators which is weakly signal dependent. The SDR curves for this case are shown in Fig. 8. Although there is noticeable distortion due to charge dump from the switches, the noise level is similar to that of the nominal (5.6448 MHz) case.

VI. Conclusions

A table-based method for simulating delta–sigma modulators has been described. The table-based method allows nonlinear circuit effects to be simulated within a reasonable amount of time. In order to generate accurate tables, capacitance-based circuit-level simulators (such as SPICE) should be avoided, and transient analyses of the switched-capacitor integrators must be properly initialized and the correct timing must be used. This method has been used to analyze the performance of a second-order delta–sigma modulator for a 14-bit digital audio application. The effects of the operational amplifier's finite bandwidth and slew rate on the performance of modulator were studied by increasing the clock rate of the modulator. The effects of charge dump were studied by increasing the size of the MOSFET switches. While these effects were successfully simulated, there are some circuit nonidealities which cannot be studied with this method, such as noise from the power supply and thermal noise. Also, while table-based methods are fast and accurate, the tables may not always provide good results. Problems can arise due to the finite precision of the circuit simulator or due to spurious errors during transient analysis.

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