Macromodels Of Digital Intergrated Circuits For High-Speed Digital Circuit Simulation

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Abstract

In digital circuit simulation, digital integrated circuits have been modeled primarily by transistor-level models or simplified lumped element models. However, there are problems with both of these approaches. The complex transistor-level models require large amounts of computer memory and have slow computation times, while simplified lumped element models do not provide the accuracy needed. Table-based macromodels provide a solution to these problems. With reduced memory requirements and faster computation times, table-based macromodels provide an alternative representation of the input and output characteristics of digital integrated circuits. This paper presents a technique for developing table-based macromodels based on measured S-parameters. Results are presented for a TTL NAND gate.

Introduction

High-speed digital circuit simulation is generally concerned with either the timing of the digital system or the transmission line effects of the digital signals. The transmission line effects are manifested as ringing and propagation delays, which distort the original signal. Simulation of the transmission line effects is generally performed using an analog circuit simulator. If the termination characteristics of digital integrated circuits could be modeled, then an analog circuit simulator could flag potential termination problems and assist with finding an optimum solution.

In general, digital integrated circuits have been modeled by either complex transistor-level models or by simple lumped element models. Both approaches have their advantages and disadvantages. Transistor-level models tend to be accurate; however, they require large amounts of memory, have slow computational times, and often have convergence problems due in part to the large number of elements. Simplified lumped element models have fast computational times and use small amounts of memory; however, their accuracy is questionable. By utilizing the advantages of both transistor-level models and lumped element models, table-based macromodels can provide an alternative solution to modeling digital integrated circuits.

This paper presents a technique to develop table-based macromodels of digital integrated circuits based on Scattering (S) parameter measurements (a technique for characterizing networks in the RF and microwave frequency range). The input and output characteristics of a TTL family of devices can be modeled with a series inductor, a series resistor, a shunt nonlinear resistor, and a shunt nonlinear capacitor. A current source can be included with the output characteristics to provide the driver characteristics of the device. A library of the device models can be created with the model components listed versus bias voltage. These models can then be incorporated into an analog circuit simulator which will predict the effects of high-speed signal propagation on printed circuit boards.

Many papers have addressed lumped-element modeling of digital integrated circuits. Greenbaum presented a macromodel of a TTL NAND gate [1]. Greenbaum models the input and the output characteristics of the TTL NAND gate with ideal current sources. The ideal current sources represent an infinite input and output impedance; however, Greenbaum's model does not account for the reactive characteristics of the device, which tend to be more predominant than the steady-state characteristics.

Glesner presents a similar model for a TTL NAND gate [2]. Glesner models the input and output characteristics with table-based current sources, which represent the nonlinear I-V characteristics of the gate. As with Greenbaum's model, Glesner's model does not account for the reactive characteristics of the device.

Theory

To illustrate the concept of input impedance, consider a transmission line of characteristic impedance Z_0 terminated in a load impedance Z_L. The load impedance Z_L is specified in terms of the characteristic impedance of the line Z_0 and the reflection coefficient Γ [3],

$$Z_L = Z_0 \frac{1 + \Gamma}{1 - \Gamma} \tag{1}$$

To determine the reflection coefficient, we use measured S-parameters. For an N-port network, the S-parameters are related to the incident and reflected voltages by the following,

$$[V^-] = [S][V^+] \tag{2}$$

Consider a two-port network shown in Figure 1. The S-parameters are related to the voltage traveling waves by [4],

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \qquad (3)$$

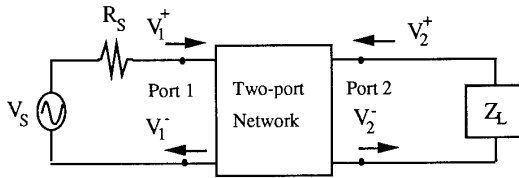$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \qquad (4)$$

Figure 1: Two-port network

S_{11} and S_{22} are analogous to the reflection coefficients at port one and port two, respectively. The impedance seen looking into port one and port two is given by Equations 5 and 6, respectively,

$$Z_{in1} = Z_o \frac{1 + S_{11}}{1 - S_{11}} \qquad (5)$$

$$Z_{in2} = Z_o \frac{1 + S_{22}}{1 - S_{22}} \qquad (6)$$

Using the impedance information obtained from S-parameters, a technique is developed based on fitting measured data to an assumed model for a family of digital integrated circuits. The assumed macromodels for a TTL device are shown in Figure 2.
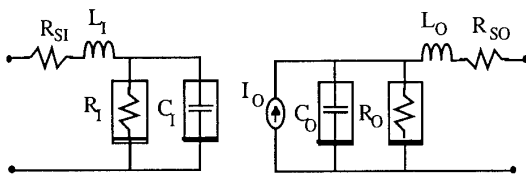
a) input characteristics   b) output characteristics

Figure 2: One-port macromodels for a TTL NAND gate

A series resistor, a series inductor, a shunt nonlinear resistor, and a shunt nonlinear capacitor model the input and output characteristics of the device. An ideal current source can be included with the output characteristics to model the driver characteristics of the device. The nonlinear resistors and the nonlinear capacitors are functions of DC bias

voltage. The inductors are linear elements, independent of DC bias voltage.

The assumed model of Figure 2 comes from the input and the output structures of a TTL NAND gate, as shown in Figure 3 [5]. The inductors, L_I and L_O, model the lead inductance due to device packaging. The series resistors, R_{SI} and R_{SO}, model the lead resistance of the package.
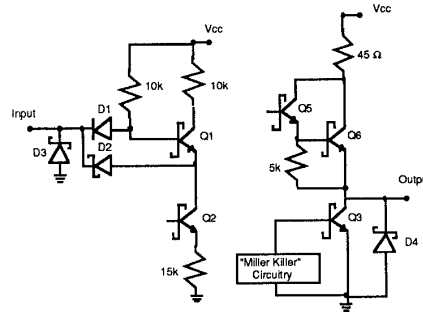

Figure 3: FTTL NAND Gate

The nonlinear input resistance of the device is due to the input diodes, the transistors Q_1 and Q_2, and the 10 kΩ base resistor of Q_1. When the device is in the low state, the diodes D_1 and D_2 are forward-biased and current flows out of the device. This current is due mostly to the 10 kΩ base resistor of Q_1. When the device is in the high state, the diodes D_1 and D_2 are reversed biased and little current enters the device. Thus, the input resistor of the model, R_I, models the change in the input current.

The nonlinear input capacitance of the device is due to the capacitance from the input diodes D_1 and D_2 and the transistors Q_1 and Q_2. The capacitance of both the diodes and the transistors changes with applied input voltage due to the dependence of the charge depletion layer with voltage. Thus, the input capacitor of the model, C_I, models the change in the input capacitance as a function of input voltage.

The nonlinear output resistance of the device is due to the transistors Q_3 and Q_6 and the 45 Ω collector resistor of Q_6. When the device is in the low state, current is sunk from transistor Q_3, and when the device is in the high state, current is sourced from the Darlington pair, Q_5 and Q_6. When the device is switching, both transistors, Q_3 and Q_6, are active. Thus, the output resistor of the model, R_O, models the change in the output current as a function of the state of the device.

The nonlinear output capacitance of the device is due primarily to the collector-to-emitter capacitance of Q_3. This capacitance is a function of the state of the device and the current through the "Miller killer" circuitry. The "Miller killer" circuitry is a transistor arrangement that removes excess charge from the base of Q_3. Thus, the output capacitor of the model, C_O,

models the change in the output capacitance as a function of the state of the device.

Calculation of Capacitors

The values of capacitors C_I and C_O are obtained from S_{11} and S_{22}, respectively. At low frequencies the impedance due to the inductors is negligible, and the capacitance can be obtained directly from the admittance of the model.

From Equations 7 and 9, the input and output admittance is found from measured values of S_{11} and S_{22}, respectively. The input and the output capacitance is calculated from the input and the output admittance, as shown in Equations 8 and 10.

$$Y_{in} = \frac{1}{Z_{in}} = Y_o \frac{1 - S_{11}}{1 + S_{11}} = G_{in} + jB_{in}$$

$$(7)$$

$$C_I(V) = \frac{B_{in}}{\omega}$$

$$(8)$$

$$Y_{out} = \frac{1}{Z_{out}} = Y_o \frac{1 - S_{22}}{1 + S_{22}} = G_{out} + jB_{out}$$

$$(9)$$

$$C_O(V) = \frac{B_{out}}{\omega}$$

$$(10)$$

where: Y_{in} = input admittance
Y_{out} = output admittance
Y_o = characteristic admittance
G_{in} = measured input conductance
B_{in} = measured input susceptance
G_{out} = measured output conductance
B_{out} = measured output susceptance
ω = angular frequency ($2\pi f$)

Circuit simulators often use charge-conservation principles, rather than capacitance, as the basis for the simulation process. Therefore, charge should be accounted for in the macromodels. The charge is obtained by integrating the capacitance over the bias voltage range, as shown in Equation 11. Simpson's rule is used to perform the integration [6].

$$q = \int_{V_o}^{V_1} C(V)\,dV + Q_o$$

$$(11)$$

Calculation of Inductors

To find the values for the inductors L_I and L_O, we measure the S-parameters of the device at various frequencies. Provided the calculations of capacitance

are correct, the impedance due to the inductance becomes predominant at higher frequencies as compared to the impedance due to the capacitance. We adjust the value of the inductance so that the S-parameters of the model closely match the measured S-parameters at each bias voltage point.

From Equation 12, the input impedance can be found from measured values of S_{11}. Equation 13 gives the input impedance of the model of Figure 2.

$$Z_{in} = Z_o \frac{1 + S_{11}}{1 - S_{11}} = R_{in} + jX_{in}$$

$$(12)$$

$$Z_{in} = R_{SI} + \frac{R_I}{1 + (\omega R_I C_I)^2} + j\left(\omega L_I - \frac{\omega R_I^2 C_I}{1 + (\omega R_I C_I)^2}\right)$$

$$(13)$$

where: Z_{in} = input impedance
Z_o = characteristic impedance
R_{in} = measured input resistance
X_{in} = measured input reactance
R_{SI} = series resistance of model
R_I = input resistance of model
C_I = input capacitance of model
L_I = input inductance of model

Thus, equating the imaginary terms of Equations 12 and 13, the input inductance, L_I, is obtained, as shown in Equation 14.

$$L_I = \frac{X_{in}}{\omega} + \frac{R_I^2 C_I}{1 + (\omega R_I C_I)^2}$$

$$(14)$$

where: X_{in} = measured input reactance
R_I = input resistance of model
C_I = input capacitance of model
L_I = input inductance of model

Analogous to the input inductance, the output inductance can be obtained from the output impedance of the model, as shown in Equation 15.

$$L_O = \frac{X_{out}}{\omega} + \frac{R_O^2 C_O}{1 + (\omega R_O C_O)^2}$$

$$(15)$$

where: X_{out} = measured output reactance
R_O = output resistance of model
C_O = output capacitance of model
L_O = output inductance of model

Calculation of Resistors

The values of the resistors R_I and R_O are obtained from the DC I-V curves of the device. The DC I-V curves are measured using an HP 6621A programmable power supply. The I-V curves are generally piecewise linear

curves, therefore the resistance can be estimated by taking the slope of the I-V curves. Thus, the values of the resistors are known at each bias voltage point.

The series resistance of the input characteristics of the model, R_{SI}, is obtained from the input impedance of the model, shown in Equation 16.

$$R_{SI} = R_{in} - \frac{R_I}{1 + (\omega R_I C_I)^2}$$

(16)

where: R_{in} = measured input resistance
R_I = input resistance of model
C_I = input capacitance of model

Analogous to the input resistance, the output resistance, R_{SO}, is calculated from the output impedance of the model, shown in Equation 17.

$$R_{SO} = R_{out} - \frac{R_O}{1 + (\omega R_O C_O)^2}$$

(17)

where: R_{out} = measured output resistance
R_O = output resistance of model
C_O = output capacitance of model

Method

The experimental setup consists of an HP 8510 network analyzer, an HP 6621A programmable power supply, and a personal computer, all interconnected via the HP Interface Bus (HPIB). A printed circuit board, which is used to test the devices, is connected to the network analyzer via coaxial cables with SMA connectors.

An automated measurement technique is used to develop the macromodels. This technique consists of HP 8510 Network Analyzer measurements, de-embedding of the measurement data, I-V curve measurements, calculation of model components, and TOUCHSTONE analysis.

S-parameter measurements are taken with an HP 8510 network analyzer. To obtain the values of the capacitors C_I and C_O of the model, S-parameter measurements are taken at 45 MHz with bias voltage applied to the input and to the output of the device from a range of 0 volts to 5.0 volts in 0.2 volt increments. The DC bias voltages are applied using an HP 6621 programmable power supply. For the output capacitance, C_O, measurements are taken for two conditions; the device in the low state and the device in the high state. The capacitors are then calculated using the procedure outlined in the theory section.

To obtain the values of the inductors L_I and L_O of the model, S-parameter measurements are taken from a range of 100 MHz to 500 MHz at a specific bias voltage point. Provided the values of capacitance at this bias voltage point are correct, the inductance is calculated based on the proposed model and the measured S-

parameters. The inductors are calculated using the procedure outlined in the theory section.

To remove the effects of the connectors from the S-parameter measurements, we use a technique called de-embedding. De-embedding is a mathematical technique to determine the effects of a test fixture on the measurements and to remove the effects of this test fixture from the measurements. The paper, "Through Symmetric Fixture: A Two-Port S Parameter Calibration Technique," describes the de-embedding technique [7].

The values of the resistors R_I and R_O of the model are obtained from the DC I-V curves. The DC I-V curves are produced with an automated measurement technique using the HP 6621A programmable DC power supply. Bias voltage is applied to the input and to the output of the device from a range of 0 volts to 5.0 volts in 0.2 volt increments. For the output resistance, R_O, the measurements are taken for two conditions: the device in the low state and the device in the high state.

The model components are calculated based on the procedure in the theory section. The model components are stored in data files in table-based format with plots provided for the following:

a) Input and output resistance versus bias voltage
b) Input and output capacitance versus bias voltage
c) Input and output charge versus bias voltage

The charge is calculated by integrating the capacitance over the bias voltage range, as shown in Equation 11.

TOUCHSTONE is a software program which performs linear analysis, interactive tuning, and optimizing of RF and microwave circuits. The optimizing routine compares measured S-parameters with a circuit model and fits the model components to the measured S-parameters. We use TOUCHSTONE to compare the calculated S-parameters of the proposed model with the measured S-parameters of the actual device.

Results

The results for the calculated model components of the input characteristics of a FTTL NAND gate are shown in Figure 5. The model components are calculated at a bias voltage of 0.6 V. Figure 6 presents a plot of the output impedance versus frequency for the device in the low state and in the high state. Figure 7 presents a plot of the forward gain (S_{21}) and the reverse gain (S_{12}) of the device.

Input Characteristics of FTTL NAND gate

BIAS (V)	R_{si} (ohms)	L_I (nH)	R_I (ohms)	C_I (pF)
.000	14.281	2.475	10000.000	6.337
.200	14.306	2.573	10000.000	5.815
.400	14.367	2.382	10000.000	5.820
.600	14.411	2.483	10000.000	5.510
.800	14.462	2.460	10000.000	5.405
.850	14.468	2.492	10000.000	5.337
.900	14.480	2.425	10000.000	5.393
.950	14.476	2.401	10000.000	5.393
1.000	14.494	2.381	10000.000	5.393
1.050	14.493	2.221	10000.000	5.560
1.100	14.489	2.327	10000.000	5.410
1.150	14.449	2.629	10000.000	5.061
1.200	13.890	2.392	1500.000	5.303
1.400	14.870	2.561	1500.000	5.171
1.600	15.458	2.245	1500.000	5.310
1.800	14.931	1.593	100000.000	5.820
2.000	14.425	1.752	100000.000	5.397
2.200	14.252	1.759	100000.000	5.256
2.400	14.153	2.265	100000.000	4.667
2.600	14.084	2.603	100000.000	4.326
2.800	14.010	2.182	100000.000	4.611
3.000	13.964	2.326	100000.000	4.438
3.200	13.909	2.177	100000.000	4.512
3.400	13.866	2.310	100000.000	4.364
3.600	13.825	2.293	100000.000	4.339
3.800	13.782	2.110	100000.000	4.444
4.000	13.746	2.331	100000.000	4.246
4.200	13.702	2.348	100000.000	4.202
4.400	13.681	2.268	100000.000	4.233
4.600	13.627	2.278	100000.000	4.202
4.800	13.605	2.297	100000.000	4.165
5.000	13.572	2.292	100000.000	4.147

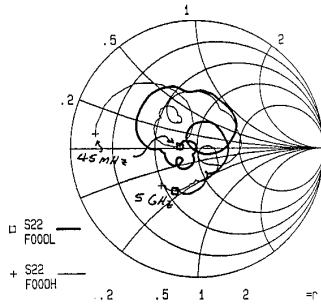Figure 5: Results of calculated model components for the input characteristics of a FTTL NAND gate.

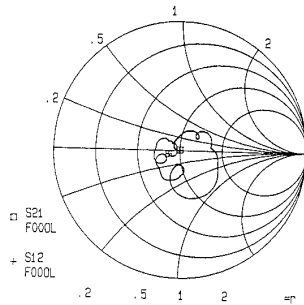Figure 6: Output impedance versus frequency of FTTL NAND gate in the low and high state.

Figure 7: Forward and reverse gain for FTTL NAND gate in the low state.

Discussion

The calculated model of Figure 5 provides an accurate representation of the input characteristics of the FTTL NAND gate. The calculated model is verified by comparing the measured S-parameters of the actual device with simulated S-parameters of the calculated model using TOUCHSTONE.

Figure 6 provides a comparison of the output impedance versus frequency for the device in the low state and in the high state. The output impedance of the device in the low state appears inductive up to 550 MHz. The ouput impedance of the device in the high state appears inductive up to 1300 GHz. The inductive effect of the output impedance is due partly to feedback effects at the output terminal.

Figure 7 provides a comparison of S_{21} and S_{12} for the output of the device in the low state. S_{21} and S_{12} are reciprocal and have low values that increase with frequency. The low values and reciprocity of S_{21} and S_{12} suggest a common path for the input and output signals. A ground inductance, which becomes significant at higher frequencies, could provide this common path.

Conclusion

This paper presents a technique for developing table-based macromodels which represent the input and output characteristics of digital integrated circuits. A table-based macromodel is presented for the input characteristics of a FTTL NAND gate. A series resistor, series inductor, a shunt nonlinear resistor, and a shunt nonlinear capacitor model the input and output characteristics of the device. A current source can be added to the output characteristics to model the driver characteristics of the device. The model for the input characteristics is verified by comparing measured S-parameters of the actual device to simulated S-parameters of the proposed model.

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