# CAD Flows for Chip-Package Coverification

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*Abstract*—A unified method is presented for layout and package design implemented within a commercial design environment that will reduce design time and enable chip-package coverification.

*Index Terms*—Chip package codesign, computer-aided design, design automation, multichip modules (MCMs), system in package (SIP).

# I. INTRODUCTION

ODAY, computer-aided design (CAD) flows for integrated circuit design are very separated from CAD flows for package design. The tools behave differently, are often provided by different vendors, and are typically based on different user interface paradigms. This leads to a number of problems and difficulties in the design of complex systems, especially with today's high performance designs and tight design cycles. First, it leaves open the scope for simple errors to propagate through to the first design iteration. For example, pin misnaming, subtle package and board mounting errors, etc. Today, there is no established approach for consistency checking across the system or module. Second, timing closure becomes much more difficult. With tight timing margins, the on-chip delay is as important as the package and board induced delays. A priori budgets do not make it easy to identify and exploit intelligent tradeoffs. In addition, such budgets do not guarantee complete signal integrity of a net that spans two chips, two packages, one board, etc. Third, lack of coordination prevents many optimizations to be discovered. A prime example would be the case where pin location reassignment improves routability at the package and board level, possibly to the extent of saving layers. Finally, with growing interest in system on package (SOP), the package will be an integrated part of the design, rather than an afterthought. Examples include RF systems with on-package passives [7], [8], as well as the concept of using the package routing resources as an extension of on-chip resources. The latter, as explored in the Seamless High Off-Chip Connectivity (SHOCC) project (e.g., [6]) was an important motivator for the work reported here.

The thesis behind the work reported here is that IC tools are sufficiently capable and flexible to solve this problem. The tools are capable of capturing the package design as well as the IC design, and to permit verification within one environment. This

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Digital Object Identifier 10.1109/TADVP.2004.841475

paper illustrates this is feasible within the context of one commercial tool set. It explains how the tool set was modified to permit capture of the physical and connectivity design of the package, to carry out layout versus schematic (LVS) verification of the complete system, and to allow automatic extraction and simulation.

This paper illustrates the feasibility and practicality of this paradigm using the Cadence commercial IC design package. It builds upon previous work of delivering CAD flows using this tool set [1] and previous work in chip package codesign [2].<sup>1</sup> In fact, it was the difficulties experienced in verifying the IC/MCM combination described in [2], [3] that motivated the work reported here. Though it illustrates this process using flip-chip multichip module (MCM) packaging, it can be easily extended to other package types. An example of an extension to simple wire-bond frame package is given at the end of the paper. All the files described in this paper are available for download.

Note that the authors are not proposing that package and board designers replace their current tools with IC tools. There are a number of practical reasons not to do this. Instead, it is suggested that it is relatively simple to import a partial or complete package and board design into the IC environment so that design tradeoffs can be easily explored and final verification performed.

This paper is structured as follows. Section II discusses the technology file that forms the core of the tool flow. Section III presents the interactive verification inside design automation (DIVA) rule deck. These are three rule files that have been created to permit designs that can be fabricated. These rules are design rule checking (DRC), extraction rules and layout versus schematic (LVS) rules. Section IV discusses a case study that was used to demonstrate the toolset that was developed. We summarize the work in Section V and conclude in Section VI.

## **II. TECHNOLOGY FILE**

By necessity, IC CAD systems are very flexible as they have to be applicable to a wide variety of IC processes, ranging from simple eight mask ones to processes requiring 20 masks or more. This flexibility is created by providing the provision to describe all the relevant data for the IC process, in a set of "technology files." No presumption of the details of the fabrication process are buried in the tools and their algorithms. The technology file defines the materials and rules we can use in the IC fabrication process. It contains the following: layer definitions; layer, physical, and electrical rules; and rules specific to individual tools and applications.

The flow described here uses these highly flexible technology files to capture package information. Essentially, the package

<sup>1</sup>Available: http://www.cadence.ncsu.edu/SHOCC\_Kit/SHOCC\_home.html

Manuscript received August 14, 2003; revised April 24, 2004. This work was supported in part by the Semiconductor Research Corporation and by DARPA, via the SHOCC consortium, and in part by the National Science Foundation.

layers are treated simply as additional IC mask layers. The rest of this section describes the process description file. Later sections describe application-specific related technology files.

The MCM metal, via, and pad layers were captured in a technology file that specifies the layer descriptions, their adjacencies, and what each via layer connects. The file also specifies minimum dimensions, grid size, etc., as well as how the layers are to be described on the screen. For example, the following extract defines the via layers and permitted connections:

;(layer1	viaLayer lay	er2)
(mcm0	mcmV1	mcm2)
(mcm1	mcmV2	mcm2)
(mcm2	mcmV3	mcm3).

One result of the technology file is the layout select window, shown in Fig. 1. This window shows the graphical mapping unique to each layer. The physical properties of the layers that are defined in the technology file are defined in a separate file known as the **Display Resource File**. The technology file and the display resource file together tell the design software how to display each layer on a specific display device.

An example of how the display resource file is coded is presented in the extract at the bottom of the page.

# III. DIVA DECK

This section deals with the DIVA rule decks. Three rule files are necessary, one each for DRC, extraction, and LVS.

## A. DRC

This rule file will permit design rule checking of the substrate and solder bumps against a geometric set of manufacturing design rules. Design rules exist so that a part can be reliably fabricated without any flaw. A designer would run the Cadence DIVA package to perform these checks.

DRC files can be written incrementally. That is, a DRC file could only check design rules for certain layers and/or certain rules only. Hence, one DRC file could be used for on-chip design and another could be used for on-substrate (i.e., off-chip) design.

The DRC deck checks for rules such as separation between same metal layer, separation between different metal layers, metal-via enclosures, minimum width of a layer, etc.

# B. Extraction

An extraction rule file allows the generation of a simulatorready netlist from a layout. It detects devices such as transistors, capacitors, solder bumps, etc., from the layout and connects them so that a meaningful circuit can be interpreted from

Edit	Help
Metal1	dg
TESTING_S	HOC
🔳 Inst 🔳 I	Pin
AV NV A	S N
🕅 metal1	dg
🔆 metal2	dg
metal3	dg
metal4	dg
cc	dg
🖉 via	dg
via2	dg
via3	dg
glass	dg
mcm0	dg
mcm1	dg
💹 mcm2	dg
/mcm3	dg
ີmcm4	dg
∭mcm¥1	dg
mcm∀2	dg
mcm¥3	dg
	dg
mcmglas	dg
nodrc	dg
nolpe	dg
pad	dg
text	dg
ires_id	dg
cap id	dq

Fig. 1. Layer select window.

the layout. In this case study, we extract long off-chip interconnects as transmission lines, and on-chip interconnect as RClines. Signal from the on-chip interconnect is passed on to the substrate through a solder pad. These solder pads are distributed uniformly throughout the chip surface. The pad layer in this case study is represented by a layer named mcm4. Whenever a metal layer and mcm4 overlap, a solder bump is placed in the extracted view. On the substrate, we have two metal layers to propagate the signal, X route (mcm2) and Y route (mcm3). The two layers are modeled as U elements (lossy transmission lines). To place the desired components (solder bumps and transmission lines) in the extracted view, the divaEXT.rul file was written.

#### C. Layout Versus Schematic

The LVS deck compares two versions of a circuit and isolates any differences. It can be used to compare two layouts,

;(DisplayName	PacketName	Stipple	LineStyle	Fill Outline)
(display	mcm0	dot4	solid	slate slate)
(display	mcm1	dot3	solid	silver silver).



Fig. 2. Driver and receiver circuit.

TABLE I New Layers Added for Package Design and Verification

Layer	Description			
mcm0	Ground plane (A shape on mcm0 signifies a hole on the layer)			
mcm1	Power plane (A shape on mcm0 signifies a hole on the layer)			
mcm2	X Metal on the Substrate			
mvmV1	Via Between mcm2 and mcm0			
mcmV2	Via Between mcm2 and mcm1			
mcm3	Y Metal on the Substrate			
mcmV3	Via Between mcm2 and mcm3			
mcm4	Top pad metal			
mcmV4	Via Between mcm3 and mcm4			

two schematics, or a layout and a schematic.<sup>2</sup> For our purpose, we use LVS to compare the extracted version of the layout and the schematic as drawn by the designer or as provided by a customer or a third party.

Such automation is particularly valuable in this application, as simple miscommunications between package and chip designers could lead to disastrous connectivity mistakes.

LVS compares the netlist from the extracted view of the layout with the netlist from the schematic that has been drawn that represents the layout. The DIVA LVS rule file is incorporated with the existing tech files and the DIVA deck so that simultaneous design and verification can be performed.

# IV. CASE STUDY—DRIVER-RECEIVER CIRCUIT

To demonstrate that the tool-set designed for this study works satisfactorily, a driver and a receiver (which is simply an inverter) circuit were connected via off-chip MCM layers. Fig. 2 (modified from Afonso *et al.* [6]) shows the driver—receiver circuit and where the interconnect attaches the two.

Signal from the driver was brought onto the substrate. The signal was propagated using the X and Y layers and was brought back on the chip to be connected to the inverter. This circuit was checked for design rule errors, extracted, and then the extracted netlist matched against the schematic netlist, thus, checking for any layout versus schematic errors.

The technology file written for the codesign and analysis of chips and substrate employing the SHOCC paradigm has a total of five additional layers and four via layers that serve as connection between these layers. New layers that are added to permit colayout of chips are given in Table I.

Layout of the test circuit was done by creating an instance of the driver and an instance of the receiver. The output of the driver is connected to the input of the receiver via the substrate layers. Metal 3 at the output of the driver is laid out in such a way such that it overlaps mcm4 layer (an SHOCC top pad layer). From there, the signal is passed through to mcm3 (which is the Y plane on the substrate) via the contact, mcmV4. The signal is then passed on to mcm2 (which is the X plane on the substrate) via the contact layer mcmV3. The signal is then brought back to mcm3 from where it is connected to mcm4 and back to metal 3 to the input of the inverter. Fig. 3 shows the layout of the driver–receiver circuit.

Once the circuit has been laid out using Cadence, we checked the validity of the design by running DRC. The rules for DRC that have been implemented in this project are from Micro-Module Systems MCM-D Technology Kit [5]. The kit is provided to support the MCM designer to accurately develop an MCM design.

For extracting the substrate layers and the solder bumps, HSPICE models were created for the X and Y metal layers modeled as U element transmission lines. The bumps were replaced by an RLC subcircuit. The extracted circuit is shown in Fig. 4.

Once we have extracted the driver-inverter circuit, we can obtain the HSPICE netlist of the extracted view using Analog Circuit Design Environment and choosing HSPICE as the simulator. Layout versus schematic program compares the obtained netlist from the extracted view of the layout with the netlist from the schematic that has been drawn that represents the layout (which can be drawn by the designer or can be provided).

Fig. 5 shows a simulation run of the obtained netlist from the extracted view. The output received is the inverted version of the input.

## V. DISCUSSION

This paper demonstrates the feasibility of using IC tools for coverification of chips and packages. The results of running these tools can be used for the tasks like the following:

- checking for design rule violations at the physical chippackage interface;
- optimizing a net or set of nets, spanning both chip and substrate, so as to meet timing or maximize performance;
- checking for correct connectivity for nets spanning the chip and package together, as well ensuring the design is consistent with the circuit model presumed.

The decks written to perform these tasks were close to 1300 lines long. No modifications were made to the execution code of the tool, nor any external new tools added.

The case study involved a power and a ground supply and it demonstrated that such a design is possible. However, can the idea be applied to a large number of signal and power planes, and is it efficient to have such a large number of power and ground planes in large designs? The answer to this question is yes. It has been demonstrated [9], [10] that power and ground lines can be designed effectively on MCMs. Now, because we have integrated circuit design package design in one tool, we can efficiently take long interconnects that overlap, off the chip, and hence, prevent crossover.

An important question is the scalability of this approach. In this Cadence installation, there are 128 user-definable layers. In

<sup>&</sup>lt;sup>2</sup>Cadence Openbook—Online Documentation for Cadence Specific Topics.



Fig. 3. The driver-receiver layout.



99



Fig. 5. Simulation of the driver-receiver circuit.

this experiment, 23 layers were used for the IC design, while ten layers were used for the package definition, leaving 95 unused layers for future expansion (e.g., a multilayer package or higher mask count IC processes). A design of up to  $27 \times 27$  cm could be accommodated with this design rule file.

It would be possible to extend this work to perform other tasks benefiting from automation. For example, chip-package nets could be sorted by criticality, filters could be written to enable selective or incremental extraction, etc. In mixed-signal designs, on-package passives could be extracted and modeled together with the IC. None of these would require changes to the CAD tool codes, just to the associated decks.

# VI. CONCLUSION

This paper demonstrates that IC design tools can be readily extended to enable the codesign and verification of high-performance chip-package systems. The IC tool extensions do not require modification of the code but of the rule decks that direct the tools. This codesign environment permits optimization of nets spanning both chips and packages, as well as verification of system-wide connectivity.

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