Buried Bump and AC Coupled Interconnection Technology

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***Abstract*—A novel physical structure, buried solder bumps, is introduced that solves the compliance problems that exist in scaling present area array technologies to ever-higher densities. In this technique, buried bumps provide dc connections between integrated circuits and substrates and ac coupled interconnections provide paths for ac signals across the same interface. This approach requires co-design of packaging and circuits and meets the growing demands for both interconnect density and bandwidth. AC coupled interconnection arrays can be built with pitches for ac signals below 100 μm and data rates of 6 Gb/s per I/O. This paper presents the physical and circuit aspects of this work as well as measured results from capacitively-coupled circuits fabricated in Taiwan semiconductor manufacturing Company (TSMC) 0.35-μm technology. Simulated results from capacitively-coupled circuits in TSMC 0.18 μm are also presented.**

***Index Terms*—Capacity-coupled circuits, coupled interconnections, integrated circuits, I/O, solder bumps.**

I. Introduction

THE DEMAND is increasing rapidly for high density, high bandwidth off-chip input/output (I/O). Though the average densities implied by the NTRS are not too different from solder bump densities achievable today, the peak I/O densities in future products are seen to pose manufacturing, test and cost barriers to existing methodologies [1].

Many researchers are addressing the need for increased I/O density by trying to find methods to manufacture cost-effective, reliable solder bump interconnections with a pitch of 100 μm or less. However, there are many known difficulties with achieving such pitches [2]–[4] A new process presented here uses buried solder bumps in conjunction with ac coupled interconnects to solve the problems introduced by continually shrinking the size and pitch of solder connections with current solder bump technologies.

In addition to increasing I/O density, a number of circuit design researchers are trying to develop methods to increase the bandwidth of each I/O by building new circuit topologies capable of multigigabits-per-second signaling. Approaches being explored include source-synchronous techniques to limit the effects of clock skew [5]; small-swing differential techniques to improve toggle rate and power-per-bit [6]; and equalization to compensate for the skin effect [6]. The ac coupled interconnection approach presented here and used in conjunction with buried solder bumps enables data rates of up to 6 Gb/s per I/O.

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II. Buried Bump Technology

A common aspect to many of the research programs aimed at increasing the density of I/Os is the dependence upon a direct, mechanical path for every I/O. One way around the mechanical limitations of decreasing the size and pitch of direct connections is to employ a contacting technology only where dc signals need to be communicated between a chip and substrate. A noncontacting technology such as capacitive coupling can then be used for signals that carry ac information. By removing the need for a direct, physical connection for ac signals, the pitch and size of the direct, mechanical connections can be greatly relaxed and the associated compliance problems of high-density direct connections can be mitigated.

In order to create separate connection types for ac and dc signals, the packaging must accommodate the needs of each signaling methodology. DC connections require a direct, physical connection, and capacitively coupled ac signals require a small chip-substrate gap on the order of a few microns. The requirements imposed by both of these interconnection technologies cannot be met by traditional packing schemes [2]. Even the most aggressive connection methodologies available today introduce a gap between the chip and substrate in the tens of microns. A novel physical structure has been developed that allows both chip-to-chip communication via ac coupled interconnects and dc paths across the chip-substrate interface.

A cross section of the structure is shown in Fig. 1. The structure consists of multiple integrated circuits (ICs) and a common substrate. Although only two trenches are shown in the figure, in practice an array of trenches is created in the substrate by using standard manufacturing processes and solder bump landing pads are created at the base of each substrate trench. Routing layers are created on the substrate surface to allow dc voltages to be brought to the solder bumps and to allow interconnection between ICs via the ac coupling elements. A portion of each ac coupling element is fabricated on the uppermost metal level of the substrate wherever ac interconnections to an IC are desired. Very large scale integration (VLSI) chips can be created with any standard CMOS fabrication process. Pads for solder bumps should be fabricated on the top metal level of the chips where dc connections are desired between the chip and the substrate. The corresponding portion of each coupling element should be fabricated on the chip surface where it is needed to ac couple signals to the substrate. Overglass openings on the integrated

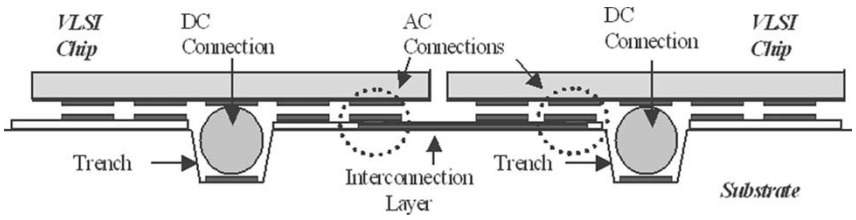
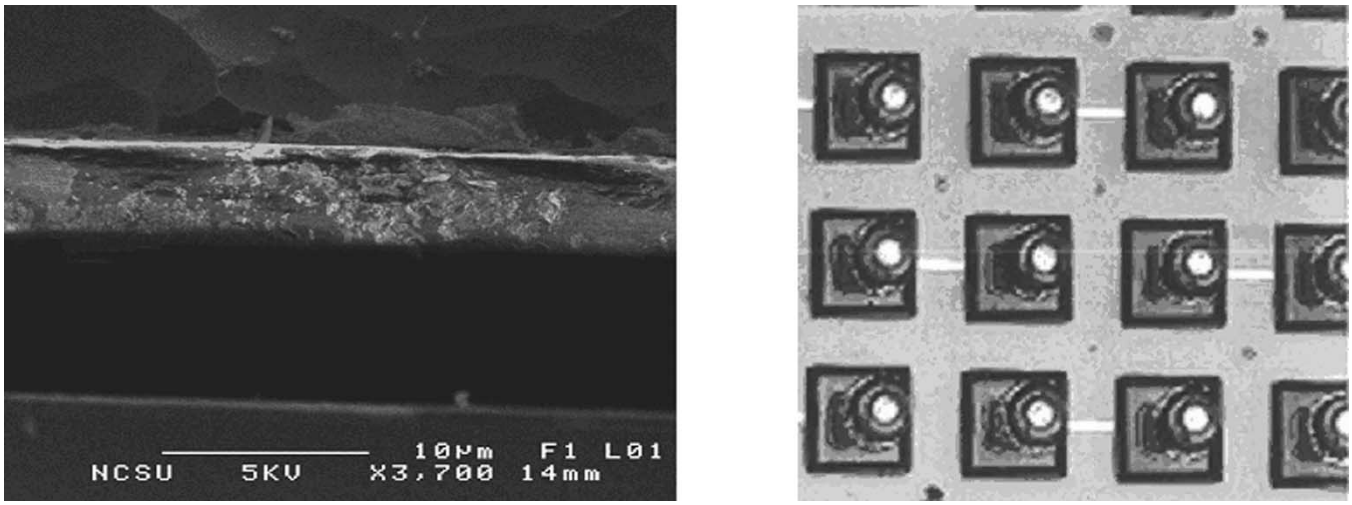


Fig. 1. Cross section of physical structure to support both buried solder bumps and ac coupled interconnections.



(a) (b)

Fig. 2. (a) Joined chip and substrate: 26-μm-deep trenches, 80-μm bump pads, 31-μm-tall solder bumps (before reflow), uniform 7.5-μm gap (after reflow). (b) Substrate image after tensile pull test separation.

circuits should be made only where solder bumps (i.e., dc connections) will be formed.

Using this structure, a bumped chip can be positioned over the substrate so that the solder bumps can be recessed into the trenches and corresponding ac coupling elements aligned. The trench depth and reflowed solder bump height are process parameters that must be tightly controlled. Once joined, the chip and substrate are separated by approximately a 2-μm gap and ac coupling can be achieved through corresponding coupling elements. As an advantage of this technique, the trench depth and the solder balls size and pitch can be made as large as necessary to provide the required compliance. All the usual advantages of solder bump assembly, such as self-alignment, are still useful in this structure. The fabrication process of the physical structure is compatible with standard CMOS processing techniques and extendible to other package materials, including ceramics and plastics.

As a demonstration, chips with coupling elements and solder bump pads were fabricated and bumped at the Microelectronics Center of North Carolina (MCNC) and the corresponding substrates with coupling elements and interconnections were fabricated at North Carolina State University (NCSU). For ease of fabrication in an R&D environment, the substrate demonstrations in this work were performed using silicon structures. The trenches on the substrate were micromachined to different depths on different experiments using an anisotropic, wet etchant. The under-bump metallurgy used for the solder bump pads consisted of a Ti–Cu stack. Scanning electron microscope images were taken of joined chip-substrate pairs and the chip-substrate gap was measured. Fig. 2(a) is an SEM image of the edge of a joined chip-substrate pair in which there was an array of 30 $\times$ 30 solder bumps in a chip footprint of 9.2 mm $\times$ 9.2 mm. Each trench on the substrate was 26-μm deep with 80-μm bump pads at each trench base. The solder height prior to joining was 31 μm. This image was taken from the center of the chip-substrate pair, but the 7.5-μm gap in this image was uniform across the entire edge of the joint.

Preliminary tensile pull tests were performed on several joined chips and substrates and it was found that the joints could withstand a pull between 50–70 lbs before tearing apart. Fig. 2(b) is an image of a section of a substrate after separation from a pull test. Although the complete array of solder bumps is not shown in the image, it was observed that all of the solder bumps across the substrate were successfully joined. It was also observed that the alignment of the chip and substrate was moved slightly off-center. This alignment can be improved by optimizing the trench size and solder bump process. Comprehensive lifetime, reliability, and tensile pull tests are planned.

III. Capacitive Coupling Overview

A buried bump structure enables capacitive coupling to be implemented for chip-chip interconnection of ac signals. When both of these techniques are used, they allow for a greater density of I/O to be fabricated and high data rates for each I/O. The physical structure presented in Fig. 1 makes possible the simultaneous creation of dc and ac coupled paths between a chip and substrate, but this structure must be considered from a circuit

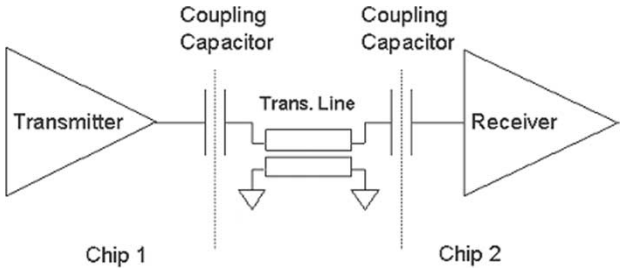


Fig. 3. Equivalent circuit view of combined buried solder bump and ac coupled interconnect physical structure.

point of view in order to analyze capacitive coupling. A basic circuit schematic for this physical structure is shown in Fig. 3. In a capacitively-coupled system the interaction between corresponding plates from the described physical structure is modeled as a series capacitance. This intentional series coupling capacitance combined with the driver/receiver shunt parasitic capacitances creates a channel from the driver to the receiver with a bandpass response. The edge rates from the driver output (dV/dt) and the accurate transmission of these sharp edges to the receiver are important parameters in passing information through this channel since the transitions are received as short pulses at the input of the receiver. Low pass filtering that occurs along this channel slows the edge rate of the transmitted signal and reduces the probability of it being correctly received.

IV. Capacitive Coupling Measurements

Measurements were made on integrated CMOS circuits with three-stage inverter drivers and receiver circuits specifically designed for recovering capacitively coupled data [7]. The tested chips were fabricated at MOSIS in the TSMC 0.35-μm technology. Each driver output was connected in series to an integrated on-chip multilevel metal capacitor—either a small capacitor (75 μm $\times$ 75 μm) or a large capacitor (150 μm $\times$ 75 μm). Also, the input of each receiver was connected in series to an on-chip capacitor—either a small or large capacitor as described above. The outputs of the transmitter capacitors and the inputs of the receiver capacitors were each connected to probe pads.

Transmitter output capacitors and receiver input capacitors were connected to each other with bond wires to test capacitive coupling over short interconnections. Fig. 4 shows the measured results from the sequence of transmitter, large coupling cap, bond wire, large coupling capacitor and receiver. The waveforms in the figure were measured at the transmitter input, at the bond wire, and at the receiver output. The input to the driver was a 3.3-V 2-GHz square wave. The total delay through the system was measured to be 212 ps. Distortion of the input waveform was an effect of impedance mismatch between the test equipment and the transmitter input. In spite of this, the receiver correctly recovered the input waveform. With NRZ data coding, the transmitter/receiver system recovered data correctly at an operating frequency of 4 Gb/s. The system was also measured and operated correctly with a 3.3-Vpp, 3-GHz square wave input, but band-limiting effects in the measurement equipment and the transistors' unity gain frequency caused the output of the receiver to be sinusoidal in shape. Simulation

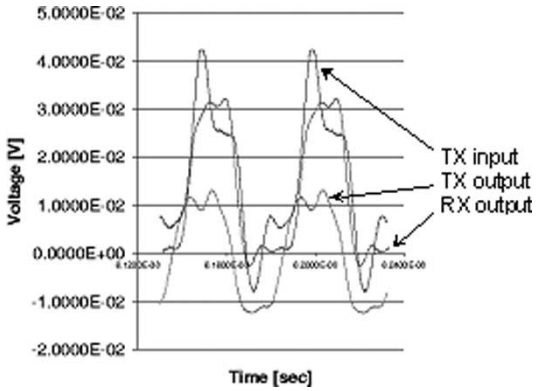


Fig. 4. Measurement results for capacitively coupled connections fabricated in TSMC 0.35 μm.

results of the system in its measurement testbed predicted this band-limiting behavior.

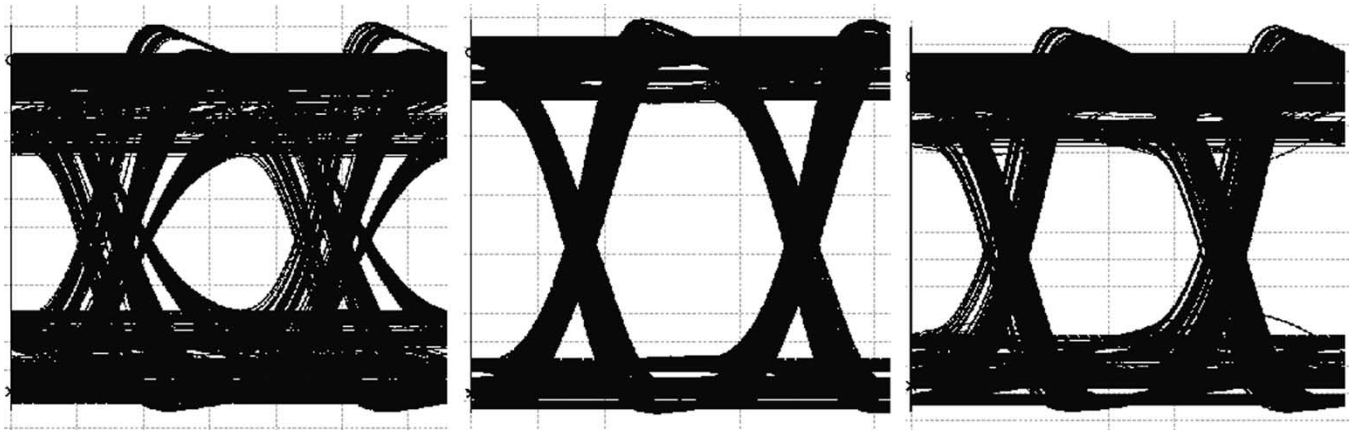
V. Capacitive Coupling Improvements

A test environment is being fabricated to measure the signal integrity (including crosstalk susceptibility) of the capacitively coupled system for random data patterns and for long interconnections up to 20 cm. Also, the 0.35-μm designs are being redesigned with differential signaling in 0.18-μm technology with 1.8-V power supply. Simulations performed with the differential version of previously fabricated circuits in the 0.18-μm technology use the W element in HSPICE to model the dc and frequency-dependent losses of the interconnections. The W element parameters were derived from standard 50 Ω microstrip lines on FR-4 PCB.

Based upon the simulation results, optimized circuits in 0.18 μm technology can achieve 6 Gb/s NRZ random data communication through 20 cm terminated chip-to-chip interconnections using a 130 fF coupling capacitor. The power dissipation will drop by 60% to less than 20 mW per I/O compared to the 0.35 μm technology and interconnection density will increase by 30% while achieving a bit error ratio (BER) below 10^{-12}. Moreover, the signal swing on the transmission lines and the coupling capacitor will drop by 90% to less than 80 mV, which means less crosstalk between neighboring chip-to-chip interconnections. It has been found that due to dc drift in the ac coupled paths, a 4–5 b encoding scheme must be employed to avoid long sequences of logic high or low from being transmitted.

Since capacitive coupling relies upon the controlled proximity of the chip and substrate surfaces, analysis has been done to understand sensitivity to the distance between the chip and substrate surfaces. It was found that the optimized circuits require a coupling capacitance of 130 $fF \pm 20$ fF to maintain an opened eye diagram at the receiver output. Fig. 5 shows receiver output eye diagram with coupling capacitances of 110 fF, 130 fF, and 150 fF. The figure shows the eye diagram of a capacitively coupled system with a terminated transmission line for a 6-Gb/s NRZ 4–5 b coded pseudorandom data with pattern length of $2^{31} - 1$.

A range of coupling capacitances exists because there is a tradeoff between using the coupling capacitor to either passively



(a) (b) (c)

Fig. 5. Eye diagram of 6 Gb/s transmission across capacitive coupled system with 86 μm per side coupling capacitors, 20 cm terminated transmission line, based on TSMC 0.18 μm/1.8 V: (a) with 110 fF C_C, (b) with 130 fF C_C, and (c) with 150 fF C_C.

compensate for the high frequency loss in the interconnection or maximize voltage swing at the receiver. Smaller coupling capacitances will close the eye diagram due to limited voltage swing. Larger coupling capacitances will close the eye due to ISI. While designed for a 2-μm gap, the range of coupling capacitance for the simulated differential circuits would allow for the chip-substrate gap to vary between 1.73–2.36 μm.

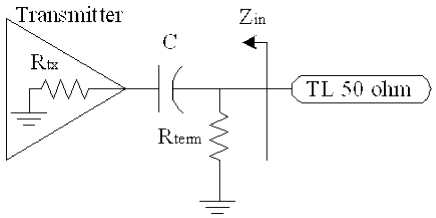


Fig. 6. Parallel termination to avoid reflections.

VI. Discussion

Two interconnection densities must be considered with a combined buried bump/ac coupled structure. AC I/O density is determined by the size and pitch of coupling capacitors. The capacitance of a coupling capacitor is found as $C = \varepsilon_o \varepsilon_r a^2/t$, where a is the length of a side of the capacitor, t is the gap between capacitor plates and ε_r is dielectric constant of the material filling between capacitor plates. Therefore, a 130 fF capacitor can be fabricated with a physical footprint of 86 μm per side with a gap of 2 μm between capacitor plates and a SiO_2 dielectric ($\varepsilon_r = 3.9$) between the capacitor plates. These dimensions would allow ac interconnections to be placed on a 100 μm pitch.

The second interconnect density to consider is the dc I/O density. By removing the need for a direct, physical connection for ac signals, the pitch and size of the direct, mechanical connections can be relaxed to achieve only the number of dc paths required for a particular integrated circuit. The International Semiconductor Technology Roadmap (ITRS) anticipates that high-performance chips in year 2010 will require 2400 signal I/O and 2400 power/ground pads in 310 mm^2 chip size [8]. Using capacitively-coupled interconnections, 2,400 signal I/O pads with 100 μm pitch will only occupy 24 mm^2 worth of chip area and will leave 286 mm^2 for power/ground solder bump connections. This will allow for solder bumps to be placed on a 345 μmm pitch. As the requirement for signal I/O density is relaxed, physically larger coupling capacitors could be used to ease the constraint on the control of the chip-substrate gap.

Each ac coupled I/O from a chip must be routed to some other chip through an interconnection on a substrate [e.g., printed circuit board (PCB)]. For long interconnections, traces on the PCB behave as transmission lines. Each ac coupling capacitor is seen in series with its transmission line interconnection, and to avoid reflections, at least one side of the transmission line must be matched. Fig. 6 shows the transmitter-side termination scheme used in these experiments. For matching, $Z_{TL} = R_{\mathrm{TERM}} \| (R_{TX} + 1/j2\pi fC)$. By properly choosing R_{TERM}, we can make $Z_{\mathrm{IN}} = 50\,\Omega$ and avoid reflections at any operating frequency. The choice for R_{TERM} however is simplified for frequencies lower than 3 GHz—since the values of coupling capacitance used in each ac coupled interconnect are small, Z_{IN} will remain almost constant and equal to R_{TERM}. Thus, we can avoid reflection in our operating frequency range with a simple termination.

The prospects for capacitively coupled interconnection improve as transistor technology improves. Communication via capacitive coupling relies on fast edge rates to transfer data across series capacitors and edge rates achievable with a three-stage inverting driver will improve as the designs are fabricated in better technologies. Also, the unity gain frequency of transistors will continue to increase and thereby allow higher data rates to be achieved. As the operating frequency increases, the capacitors can be made smaller while still allowing the possibility of an impedance-matched interconnection. The use of underfills in the physical technology could introduce a dielectric constant larger than SiO_2 for the capacitors and allow the size of a coupling capacitor to shrink further still. Crosstalk can be mitigated in two important ways. First, the power/ground structure provided by the physical technology can be designed to make one or more power and ground connections available for every signal path. Also, the use of more advanced CMOS process technologies will allow for reduced voltage swing on the interconnections which will help to mitigate the effects of crosstalk.

AC coupled interconnects can be thought of as connecting a transmitter to a receiver through a band-pass channel. The pass band generally covers at least a decade of frequency and the cut-off frequencies can be manipulated by changing the details of the physical structure. Optimization of the physical structure, the circuit topologies used for the transceiver and the frequency response of the band pass channel is ongoing.

The nature of high-density I/O requires high-density wiring. However, in the case of ac coupled interconnect, the package wiring does not have to match the pitch of the IC wiring. The substrate demonstrations in this work were performed using silicon structures; however, this approach can be used in ceramic or plastic packaging as well. For example, holes could be punched in the top layer of a ceramic package, when in green tape form, to permit later solder ball attachment. So far, no fundamental barrier to exploitation has presented itself.

VII. Conclusion

A new approach to building 100 μm pitched arrays of 6 Gb/s/per pin digital chip-to-package connections has been developed in which digital signals are carried using noncontacting series capacitance structures. DC signals are transmitted between chip and substrate via buried solder bumps, and these recessed solder bump connections have the additional function of controlling the gap and the alignment between the chip and substrate.

By using both ac coupled and dc connections in the same chip-substrate interface, high I/O bandwidths and densities can be achieved without the mechanical, compliance and rework complexities typically associated with fine pitch interconnects. NRZ-tolerant transceiver topologies are being optimized to best exploit this technology. Experiments have been performed to demonstrate the feasibility of both the buried solder bump concept and the overall interconnect circuit structures.

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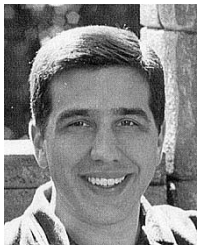

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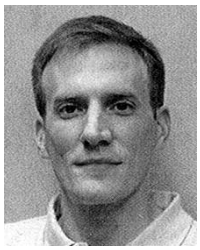

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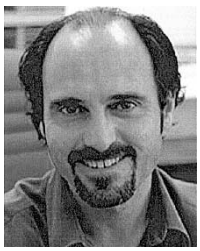

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Dr. Franzon received the National Science Foundation Young Investigators Award in 1993, was selected to join the North Carolina State University Academy of Outstanding Teachers in 2001, and was selected as a Distinguished Alumni Professor in 2003.