Thermal Simulation of Heterogeneous GaN/ InP/ Silicon 3DIC Stacks

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Abstract—**Integration of materials such as GaN, InP, SiGe, and Si is a natural extension of the 3D-IC perspective and provides a unique solution for high performance circuits. In this approach, application of a component is no longer dependent on semiconductor material selection. In this paper, preliminary results are presented which examine the thermal performance of the technology. A thermal analysis prototype solution in Mentor Graphics™ Calibre® provides surface heat maps based on IC layout, material property, and geometric configuration files. Chiplets are connected by heterogeneous interconnect (HIC). Differences in thermal performance of GaN and InP chiplets are explored by varying the number of HICs. Two methods for building up the model of a test chip are compared. One method uses custom scripts to place discrete blocks in the model to represent HICs, while the other uses thermal material properties extracted from the layout. Measurements presented confirm simulated results.**

Keywords— ***thermal simulation; 3D-IC; GaN HEMT; heterogeneous integration; thermal modeling***

I. Introduction

A goal of the Diverse Accessible Heterogeneous Integration (DAHI) DARPA program [1] is to build capability in integrating various semiconductor materials into single component chips. The method of interconnecting the IC sub-circuits of the differing technologies is by use of the Heterogeneous Interconnect (HIC) structure. Similar to a through-silicon via (TSV), a HIC is a vertical metal structure which passes through layers of the IC to connect to metal layers and thus join separate chiplets.

This paper presents a comparison of different methods for thermal simulation of the HICs in a DAHI chip. Similar finite element methods have been employed for 3D-ICs [2]. The first method uses an automated material property extraction from a layout file. The extracted thermal properties are then used to create a layer of HICs in the model stackup. In the second method, scripts are used to identify HIC locations and thermal source locations. The locational information is then used to create a separate simulation block for each shape. With the last method, HICs can optionally be countersunk into the above and below bulk material, thus increasing the level of three-dimensional detail for this implementation. The same capabilities exist for creating models with complete detail in the first extraction method.

The HIC is judged to be an area of focus for simulation because of its importance in joining the technologies, mechanical complexity, and its role as a thermal conduit and bottleneck providing the only heatsinking ability to the chiplets. These simulation methods are compared by temperature result accuracy or agreement, ease of setup, and result resolution.

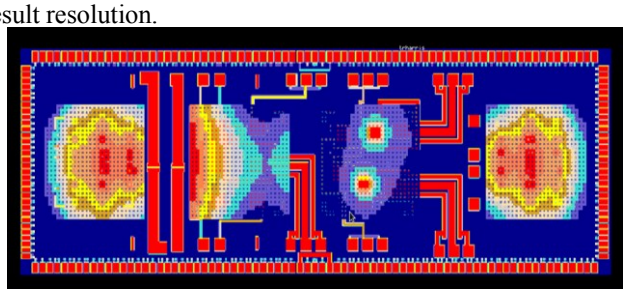

Fig. 1. The simulated thermal heat map of four chiplets superimposed over the thermal conductivity map of the carrier CMOS chiplet.

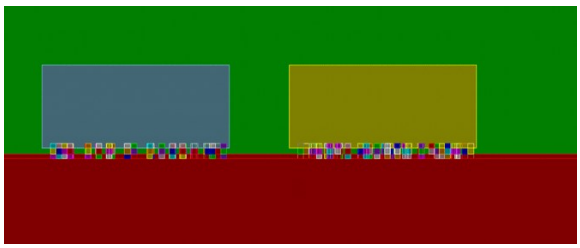

Fig. 2. A profile view of the chiplets with HICs placed using the Instance Discovery method

II. Thermal Simulation

A number of experiments have been performed in order to compare performance differences between semiconductor materials as well as to compare with measurements of a physical test chip currently in fabrication. A detailed model of

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the test chip has been created for simulation.

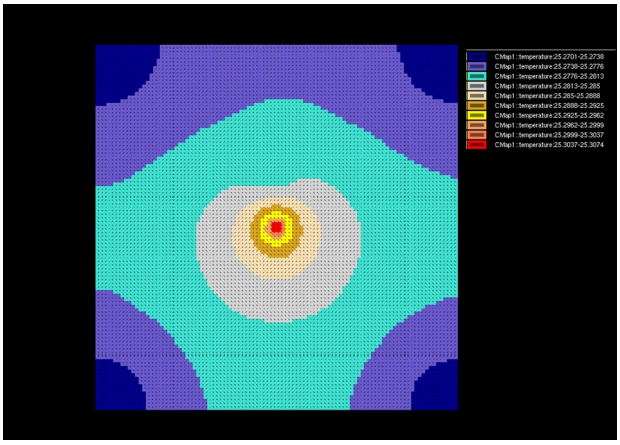

Fig. 3. Simulation results showing a thermal map of an InP HBT with four HICs along the top of the device.

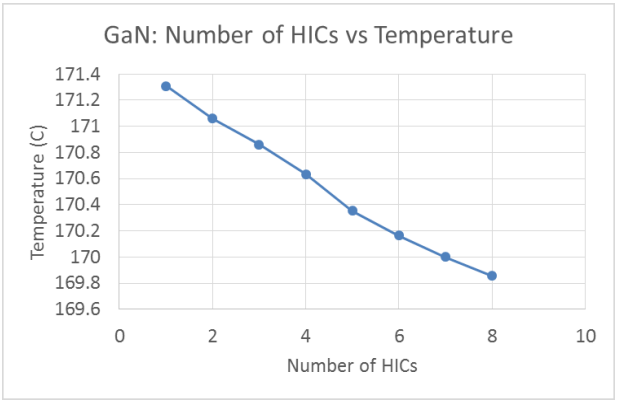

Fig. 4. GaN HEMT maximum temperature as the number of HICs surrounding the device is increased

A. Thermal Property Extraction and Instance Discovery

The HICs have been recognized as an area of importance for thermal and mechanical performance. Attention should be given to modeling the HIC interconnect of the high temperature GaN and InP chiplets to the CMOS carrier chip. Two methods for creating the model are presented here. Effective thermal property extraction (EFFP) is a feature of the Mentor Graphics Calibre prototype which can build a thermal property file based on a layout and files specifying material layers and properties. The thermal property file can then be assigned for use in a block in the model. In this case, the metal material properties are used for the HIC while the appropriate dielectric properties are used for the space between the HICs, chiplets, and CMOS die. The resulting block is used as an interposer layer in the model. Simulation results from this method are shown in Fig. 1. In this figure, the color thermal map results of the GaN and InP chiplets are superimposed over a colormap of the *x*-thermal conductivity of the CMOS chip. The portion of the metal interconnect layout with high conductivity is shown in red for the extracted area. This model shows a higher level of detail than currently employed in the second method where only HICs are placed.

In a second method for building the DAHI model called Instance Discovery, the flow starts by a using a script to scan the layout which saves size and location of each HIC. HIC instances are identified by matching the cell names. The output data are then parsed by another script and output to the Calibre configuration file in order to create a block for each HIC instance. In order to create a more detailed model, each HIC is divided into three pieces: an upper, middle, and lower section. The segmentation is done because the vertical structure of the interconnect physically extends into the CMOS and connecting chiplet. The increased level of detail for this specific implementation affords the Instance Discovery method better accuracy. However, it is expected that each chiplet will use EFFP in the future to more accurately model the die by taking into account the metalization of interconnects and vias. With chiplets extracted by EFFP, HICs will join the internal metal layers within each adjoining block. Each model building method, EFFP and Instance Discovery, uses the Instance Discovery scripts for identifying transistor sizes and locations in the layout and in turn writing the power map configuration files. Comparing the results of the EFFP HIC layer against the Instance Discovery method shows agreement, with active layers ranging up to 180 ºC.

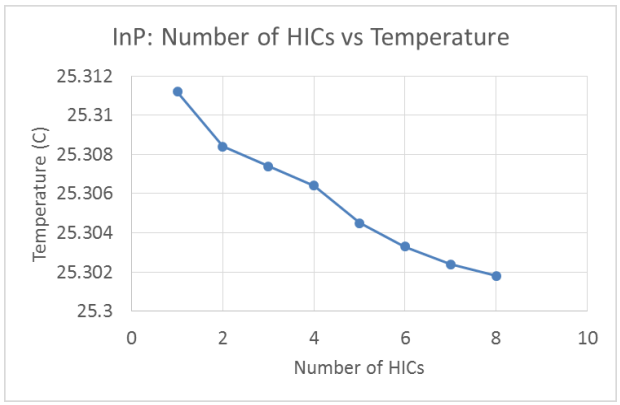

Figure 5. InP HBT maximum temperature as the number of HICs surrounding the device is increased.

B. HIC Number Variation Comparison of InP and GaN

The number of HICs surrounding a heat producing device was varied in order to study the heat sinking effects and to compare the thermal properties of GaN and InP. For each material, a HIC was added to the model near the transistor for each data point, in addition to HICs added to the four corners of each device, as per design rules to add mechanical stability. One to eight HICS were sequentially added around the device. Each additional HIC adds an additional thermal path in parallel to the heatsink as defined by simulator boundary conditions and thus lowers the maximum device temperature. The average temperature of the chiplet is further reduced. The geometry of the power injection area for each transistor is based on standard sized kits available with the area for InP being 0.45 µm x 0.8 µm with static power of 250 µW and the GaN being 72 µm x 32 µm with a power of 250 mW.

An example of the output of the thermal simulator is shown by the thermal map in Fig. 3. A single InP chiplet with a single test transistor from the test chip model is highlighted. The remaining three chiplets and CMOS carrier are not visible in this figure for clarity but are required for simulation completeness. Smaller slices of sections of the model cannot be omitted from the simulation to decrease simulation time due to the heatsinking effects of the thermal mass. However, reducing the detail of the model is possible in the far-field without changing results. To achieve speed up for this test, far field chiplets were attached to the CMOS carrier by an attachment layer with thermal conductivity properties approximating a non-solid array of HICs or c4 bumps. Fig. 3 shows that temperatures are cooler along the top of the thermal map. This pattern is due to the fact that there are four HICs placed north of the device, with none to the south, other than the corner HICs, which leads to the asymmetric temperature profile.

In Figs. 4 and 5 the maximum temperature vs. number of HICs simulated is shown for GaN and InP, respectivly. These simulations require approximately 70 mins for each data point. A one-dimensional analysis of the injected power, geometry of the semiconductor stackup, and thermal resistance has shown that these simulation results are within an expected range. Without thermal measurements of the chip in fabrication, accurate calibration of the simulator is not yet possible. Verification is possible using calculations for worst case and best case temperatures based on the geometries above and thermal conductivities.

For the InP chiplet, an estimate of thermal resistance can be calculated in a method similar to [3, 4] by using $\theta = L / Ak$, where θ is thermal resistance, L is the length of the path to thermal ground (device thickness), A is the area of the region being considered, and k is the thermal conductivity of the material in W/(m ºK). Ambient temperature specified for each model in Figs. 4 and 5 is 25 ºC. Using $T = P\ \theta$, where T is temperature, and P is power, a temperature rise of 0.3 to 3 ºC is expected. A similar calculation using the appropriate values for the conductivity of SiC, GaN provides a range for Fig. 4.

There are several factors contributing to the differences of HIC effects on the GaN and InP semiconductor materials. The factors include that SiC is a superior thermal conductor to InP, the InP chiplet is relatively thinner than the SiC chiplet, input power for the GaN device is a magnitude higher, and chiplet orientation differs.

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III. Measurments

For validation of the thermal models, measurements of the

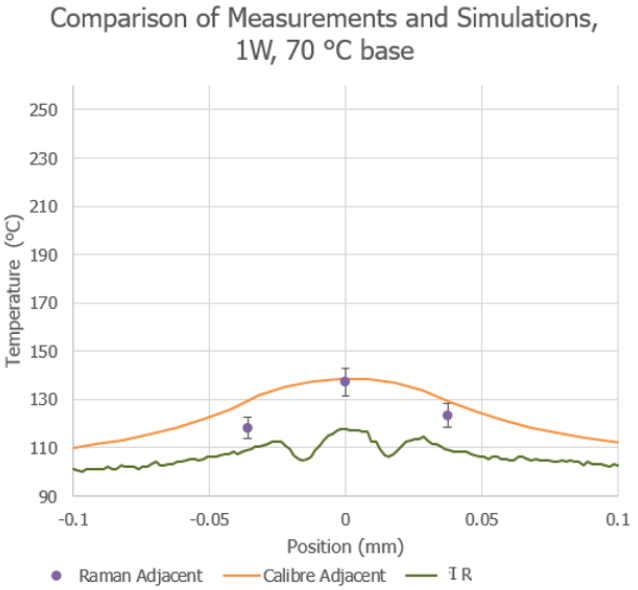

Figure 6. Thermal simulation data of the gate are compared against IR and Raman measurements.

powered GaN transistor were taken using a QFI Infrascope at varying power density levels of operation. The QFI system is designed to calibrate for differences of emissivity of materials by use of a calibration image while the chip is heated to an offset temperature. Here, 70 ºC was used as the base temperature. GaN, SiC, and Si in the DAHI stackup are visibly transparent and partially transparent to IR wavelengths. Therefore, thermal Raman measurements were used as a second method of model validation. Figure 6 shows that IR microscopy under-predicts temperatures taken at the gate fingers by 5 – 10 ºC.

IV. Conclusion

Two approaches for creating a composite 3-D model of a DAHI test chip have been discussed. In one approach, the property extraction method, the thermal conductivities of the specific layers are extracted and used as a property map for a large block. The second approach identifies desired HIC instances and transistor active regions, and in turn creates 3-D block shapes and corresponding power maps. Both methods accomplish the same task of creating a model which includes HIC locations to connect the chiplets to the silicon chip. The EFFP method is optimized to be 5x faster than the instance discovery method, and both simulation methods provide matching thermal results.

The techniques show promise for use in the DAHI design flow, particularly the extraction method because it is foreseen that each chiplet including the CMOS chip will be simulated in extracted form to account for the metalization in the die, thus building the model will be simplified. The instance discovery script from the block placement method is still useful for creating the heat maps based on the transistor active region data. The Instance Discovery method can have useful facility for building the chiplets of the model, power map files.

Results were presented comparing GaN and InP transistor thermal performance as the number of local HICs nearby the device are varied. These simulations were verified through thermal IR and Raman measurements. These tests build confidence in the model, show the heat sinking effects of the HICs for each material, and are also valuable for building designer intuition.

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