An Analysis of Subthreshold SRAM Bitcells for Operation in Low Power RF-only Technologies

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***Abstract*—Current RFID systems rely on the RF transciever to transmit information and convert RF power to DC to operate any integrated digital circuits. Research investigating the application of RF signals directly on digital CMOS circuits without RF-DC conversion is an emerging area for RFID technologies. One crucial digital circuit for most RFID systems is memory, needed for storing operational instructions and sampled data. An in-depth study and comparison of subthreshold SRAM bitcells has been conducted to analyze how such memories will function in a subthreshold RF-only regime without the need for RF-DC conversion. Several SRAM cells were chosen for conversion into the RF-only family and measured against several metrics, including highest performance at lowest operating voltage, power consumption, and static noise margins (SNM). Including RF supply transistors, an 18-T subthreshold RF-only bitcell is proposed, capable of operating at a data rate of 100 kHz at V_{RF} of $200\,mV_{RMS}$.**

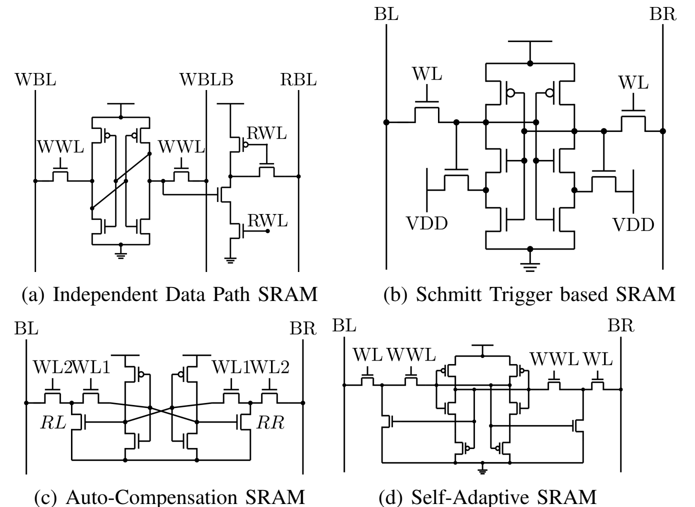
I. Introduction

Research into possible technologies for the subthreshold operation has grown drastically in recent years with the demand for low-power, ultra-low-voltage micro-systems. Operation of CMOS circuits below threshold voltage offers many benefits including low dynamic and static power and reduction of short-circuit power [1]. Such benefits are crucial for CMOS digital systems and integrated circuits (ICs), such as sensors, which rely on limited power sources without a need for high performance. Radio-frequency identification (RFID)sensors are good examples of systems that could benefit from subthreshold operation. Typically, RFID systems include CMOS digital systems which serve more dedicated tasks. Even if implemented in subthreshold, these back-end digital systems often rely on the RFID front-end to capture RF power for DC conversion [2].

Subthreshold RF-powered CMOS digital circuits without RF-DC conversion have been introduced in [3]. Such CMOS circuits are directly powered by the RF source, allowing for deep subthreshold operation (as low as $160\,mV_{RMS}$), as well as operation over a large range of RF frequencies [3]. This paper presents an RF-powered subthreshold CMOS SRAM bitcell for use in RF-only digital systems.

II. Subthreshold DC SRAM Bitcells

For subthreshold operation, several different mechanisms have been introduced to SRAM bitcells to decrease the required operating voltage and possible leakage paths [4], while increasing cell stability through improvement of static noise margins (SNM) [5] and variation process tolerance [6]. To minimize the operating voltage, the 10-T bitcell presented by Kim et al. [7] (shown in Fig. 1a) increases the channel length of the write access transistors to utilize the reverse short channel effect (RSCE) for stronger drive currents. To decrease leakage, this cell utilizes a decoupled read path, isolated from the storage nodes, which also improves read noise margins [7]. The 10-T Schmitt Trigger bitcell presented by Kilkarni et al. [8], shown in Fig. 1b utilizes Schmitt trigger action to reduce leakage, as well as a built-in feedback mechanism to increase the switching threshold of the node transitioning from “1” state to “0” state to improve process variation tolerance. This feedback mechanism also works to boost read SNM by reducing the read failure probability [8].



(a) Independent Data Path SRAM (b) Schmitt Trigger based SRAM (c) Auto-Compensation SRAM (d) Self-Adaptive SRAM

Fig. 1. Schematics of SRAMs compared in DC and RF subthreshold regimes: (a) is the bitcell with an independent data leakage path presented in [7], (b) is the Schmitt Trigger based SRAM presented in [8], (c) is the fully-differential read SRAM with auto-compensation presented in [9], and (d) is the differential read SRAM with self-adaptive leakage control presented in [10].

Many subthreshold SRAM designs trade size for a decreased leakage path, such as the 10-T bitcell presented by Chang et al. [9] (shown in Fig. 1c), which introduces additional access devices to isolate storage nodes from bitlines during a read for boosted read noise margins. This bitcell also implments an auto-compensation mechanism which automatically compensates imposed noise disturbing the cell to hold the storage nodes at their proper values, as well as a virtual ground (VGND) scheme to reduce the data retention ability of cell during a write operation [9]. The 10-T bitcell presented by Na et al. [10], shown in Fig. 1d also introduces additional access devices while utilizing a re-configurable operating principle (wordline boosting) to maintain reliability and reduce leakage current. Pseudo-writes, or false-writes, occur when unselected cells undergo a write as the WWL signal is asserted while the write bitlines are precharged to V_{DD} [7]. The additional access devices introduced in Chang et al. [9] to isolate the storage nodes during a read create the requirement that both WWL and WL signals to be asserted for a write to occur, solving the pseudo-write issue within the bitcell.

III. Subthreshold RF-only SRAM Bitcells

Selected bitcells were first simulated for the DC-regime in the IBM $0.13\,\mu m$ bulk CMOS process, and then implemented for the

TABLE I

SIMULATED READ AND HOLD SNM VALUES FOR SRAM BITCELLS, WHERE DC V_{DD} IS 250 mV AND V_{RF} IS 250 mV_{RMS}, 100 MHz.

Cell	DC Read	RF Read	DC Hold	RF Hold
[7]	64 mV	55 mV	65 mV	55 mV
[8]	35 mV	31 mV	23 mV	28 mV
[9]	61 mV	57 mV	60 mV	56 mV
[11]	63 mV	34 mV	62 mV	43 mV

TABLE II

SIMULATED WRITE SNM VALUES FOR SRAM BITCELLS, WHERE DC V_{DD} IS 250 mV AND V_{RF} IS 250 mV_{RMS}, 100 MHz.

Cell	DC Write	RF Write
[7]	91 mV	112 mV
[8]	137 mV	137 mV
[11]	247 mV	224 mV

RF-only regime in the same process. Each bitcells RF characteristics were compared to its own DC characteristics to understand the effect RF has on voltage scaling, power, noise margins, and performance of the bitcell. For analysis in the RF-only regime, simulations were performed that varied the RF signal's strength from 160 mV_{RMS} to 800 mV_{RMS} and its frequency from 13.57 MHz to 915 MHz.

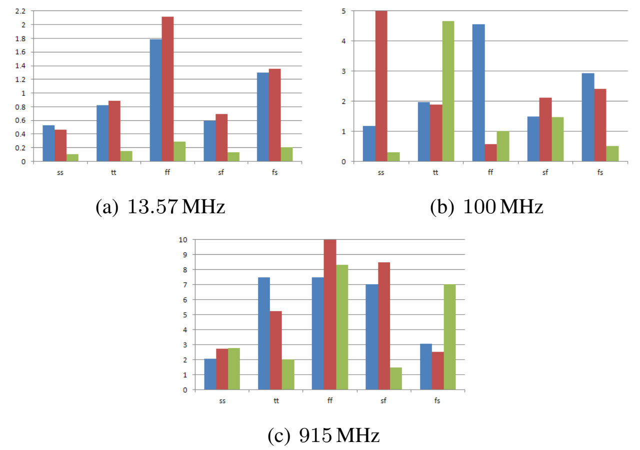
Table I is a comparison of the read and hold noise margins simulated for an operating voltage of 250 mV DC and 250 mV_{RMS} RF. This shows that when converting from the DC regime to the RF-only regime, read SNM decreases an average of 20%, while hold SNM decreases an average of 18%. Table II is a comparison of the write noise margins simulated for an operating voltage of 250 mV DC and 250 mV_{RMS} RF. This shows that on average, write noise margins vary by 10% from DC to RF.

As the RF operating voltage is scaled from 500 mV_{RMS} to 300 mV_{RMS}, all bitcells simulated in RF show a 10x or more decrease in data speed with a typical 3:1 sizing ratio between the PMOS and NMOS devices. At an operating voltage of 225 mV_{RMS}, all bitcells simulated show correct functionality at a data speed of 100 kHz. A huge focus of process variation tolerance is on reliability of the bitcell in subthreshold, but for this work, emphasis was placed on how process variation affects power and performance. To examine this, the cells were simulated with varying RF operating voltages and frequencies over the various process corners. The results showed that as the RF signal frequency is increased, the average power consumed increases, as shown in Fig. 2 for a data speed of 100 kHz and an operating voltage of 300 mV. The results also showed that as the process device speeds increase, so does the average power consumed, as well as an increased percentage for device failure and a need for a decreased data speed.

For further study in the RF-only regime, the 10-T bitcell with a decoupled read path presented by Kim et al. in [7] was selected based on its higher noise margins and moderate power consumption at lower RF operating voltages, as compared to the self-adaptive [10] and the robust Schmitt trigger based [8] bitcells. The differential read bitcells with auto-compensation [9] and bit-interleaving [11] require techniques such as word line boosting and differential sense amplifiers to boost voltages to full swing voltages or higher to obtain low power and high noise immunity. Such techniques were out of the scope of this work.

IV. AN 18-T RF-ONLY SUBTHRESHOLD SRAM BITCELL

The schematic of the proposed 18-T subthreshold RF-only SRAM bitcell based on the 10-T subthreshold DC SRAM bitcell presented in



(a) 13.57 MHz (b) 100 MHz

(c) 915 MHz

Fig. 2. Changes in average power consumed per bitcell operation, in units of nW, over the IBM 0.13 µm Bulk CMOS process for a V_{RF} of 300 mV_{RMS}. Bitcells [7], [9], and [10] are represented, respectively, in each graph.

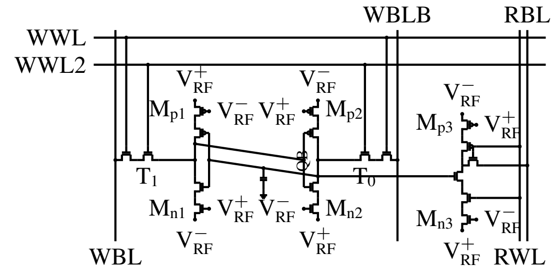
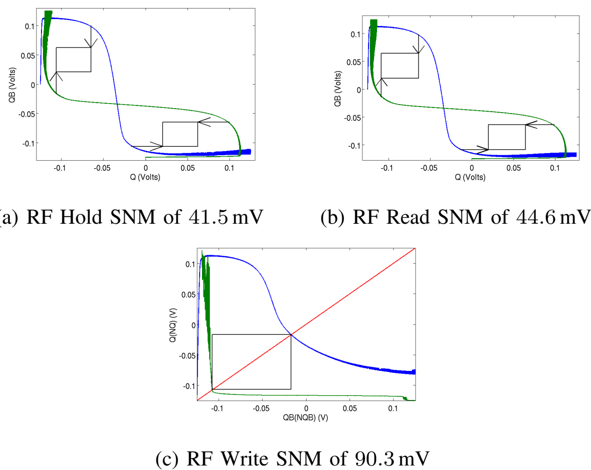


Fig. 3. 18-T RF-only bitcell, modified from [7].

[7] is shown in Fig. 3. Two additional access transistors, T_0 and T_1, are added as a solution to the pseudo-write issue instead of the row-dependent writeback scheme presented in [7]. Transistors T_0 and T_1 are asserted by the second wordline signal, WWL2. Thus, to perform a write, both wordline signals, WWL and WWL2, must be asserted as presented in [10].

Six RF supply-transistors (shown as M_{p1}, M_{p2}, M_{p3}, M_{n1}, M_{n2}, and M_{n3} in Fig. 3) are added to the bitcell. These devices supply current from the RF signal to the digital circuit when on, and help minimize leakage from the storage nodes when off [3]. Since the RF source is at a higher frequency than the CMOS data rate, a capacitor is placed on the internal storage node QB to preserve the partial computation during the dead time of the RF signal, when the RF voltage is too low to power the circuit [3]. For this bitcell, it was found that when operating below 250 mV, the leakage is minimal and the capacitor is unnecessary. But when operating at higher voltages, such as above threshold, the leakage during the RF dead time is high and the capacitor is required for proper functionality. Phasing of the storage node supply transistors (M_{p1}, M_{p2}, M_{n1}, M_{n2}) is shown in Fig. 3. Phasing allows for evaluation of the logic circuit to continue during both positive and negative phases of the RF signal by keeping the stored value valid during each opposing phase [3].

At a V_{RF} of 250 mV_{RMS} and a V_{RF} frequency of 100 MHz, the simulated hold SNM value of the bitcell is 41.5 mV, shown in Fig. 4a. The simulated read SNM is 44.6 mV, and the simulated write SNM is 90.3 mV, also shown in Fig. 4c. The addition of the access devices, T_0 and T_1, without adding differential access devices (transistors RR and RL in Fig. 1c), which serves to isolate the storage nodes during



(a) RF Hold SNM of 41.5 mV

(b) RF Read SNM of 44.6 mV

(c) RF Write SNM of 90.3 mV

Fig. 4. For a V_{RF} of 250 mV_{RMS}, 100 MHz, (a) shows the hold SNM, (b) shows the read SNM, and (c) shows the write SNM for the proposed 18-T RF-only SRAM bitcell.

reads and holds, induces the drop in static noise margin values seen above. These devices were not added in this work since reads are performed via the data independent leakage path from node QB.

V. Conclusion

A subthreshold, RF-powered 18-T CMOS SRAM bitcell has been presented for use with ultra-low-voltage, RF-only digital circuits, without the need for RF-DC conversion. Simulated in the IBM 8RF 0.13 µm process, the proposed bitcell is capable of proper functionality at a V_{RF} as low as 170 mV_{RMS}, and an average power of 1.659 nW at an operating voltage of 200 mV_{RMS}, 100 MHz.

References

[1] S. Fisher, A. Teman, D. Vaysman, A. Gertsman, O. Yadid-Pecht, and A. Fish, "Digital subthreshold logic design - motivation and challenges," in *Electrical and Electronics Engineers in Israel, 2008. IEEEI 2008. IEEE 25th Convention of*, dec. 2008, pp. 702 –706.

[2] S. Venkataraman, C. Hutchens, and R. Rennaker, "Rf-front end for wireless powered neural applications," in *Circuits and Systems, 2008. MWSCAS 2008. 51st Midwest Symposium on*, aug. 2008, pp. 682 –685.

[3] P. Gadfort and P. D. Franzon, "RF-only Logic Circuits," in *2011 Sub-Threshold Conference*, September 2011. [Online]. Available: http://www.musyc.org/pubs/282.html

[4] M. Sharifkhani and M. Sachdev, "Sram cell stability: A dynamic perspective," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 2, pp. 609 –619, feb. 2009.

[5] B. Calhoun and A. Chandrakasan, "Analyzing static noise margin for sub-threshold sram in 65nm cmos," in *Solid-State Circuits Conference, 2005. ESSCIRC 2005. Proceedings of the 31st European*, sept. 2005, pp. 363 – 366.

[6] M.-E. Hwang and K. Roy, "A 135mv 0.13 uw process tolerant 6t subthreshold dtmos sram in 90nm technology," in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, sept. 2008, pp. 419 –422.

[7] T.-H. Kim, J. Liu, J. Keane, and C. Kim, "A 0.2 v, 480 kb subthreshold sram with 1 k cells per bitline for ultra-low-voltage computing," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 2, pp. 518 –529, feb. 2008.

[8] J. Kulkarni, K. Kim, and K. Roy, "A 160 mv robust schmitt trigger based subthreshold sram," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 10, pp. 2303 –2313, oct. 2007.

[9] M.-T. Chang and W. Hwang, "A fully-differential subthreshold sram cell with auto-compensation," in *Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference on*, 30 2008-dec. 3 2008, pp. 1771 –1774.

[10] B. Na, X. Chen, Y. Jun, and S. Longxin, "A differential read subthreshold sram bitcell with self-adaptive leakage cut off scheme," in *SOC Conference (SOCC), 2010 IEEE International*, sept. 2010, pp. 455 –460.

[11] I. J. Chang, J.-J. Kim, S. Park, and K. Roy, "A 32kb 10t subthreshold sram array with bit-interleaving and differential read scheme in 90nm cmos," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, feb. 2008, pp. 388 –622.