Design of a Rectifier-Free UHF Gen-2 Compatible RFID Tag using RF-Only Logic

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***Abstract*— AC-DC rectifier and storage capacitors take up 25% or more of chip area for cost-sensitive passive RFID tags. In this work, we show that these components can be eliminated by utilizing a RF-only circuit structure. Therefore, the chip would be smaller and cheaper. RF-only logic permits digital operations to be performed from an AC, rather than DC, power supply. An UHF Gen-2 compatible RFID tag is designed using the RF-only logic. Powering and communication solutions in direct ASK carrier powered scenario are developed. RF front-end circuits are designed in RF-only fashion and a standard cell library of RF-only logic is developed and tailored for this application. The RFID tag is implemented in a 0.13 µm CMOS technology. The tag dimensions are 0.6 mm × 0.3 mm and its sensitivity is 0 dBm at RF amplitude of 500mV in simulation. The same methodology can be applied to enable lower RF amplitude implementations that trade off area for sensitivity.**

***Index Terms*—RFID tags, Logic circuits, Rectifiers, AC power supply, Area efficient.**

I. INTRODUCTION

Radio Frequency Identification (RFID) enables asset tracking, supply chain management, payment system, security and access control. Due to the advantages of long operating range and low cost, the EPC Class 1 Generation 2 compatible RFID tags working at ultrahigh-frequency (UHF) have attracted considerable attention. One of the major constraints that limit wider adoption of RFID technology is the per-tag cost. Currently, the tag cost is roughly 10 cents based on volume and transponder specifications [1]. However, the cost of RFID tags needs to be further reduced if they are to replace barcodes on inexpensive items for labelling.

A typical passive RFID tag harvests RF power by rectifying the received AC signal into a DC voltage with a multi-stage rectifier and boosting its value with a charge pump [2] [3] [4]. This DC voltage is regulated to a stable supply voltage by the regulator, followed with large storage capacitors to reduce voltage spikes and ripples. The state-of-the-art powering solution takes up considerable chip area. Inspecting RFID chip layouts usually indicates that these functions take up 25% or more of the chip area [5] [6]. It would be desirable to power the RFID tag directly with RF signal without AC-DC rectifying, thus saving the area and cost. Briole [7] proposed a dual phase AC powered logic circuit to eliminate the need of rectifiers, but the doubling of transistor counts and overhead of transmission gates does not lead to an area savings. Wenck [8] proposed to power the conventional CMOS digital circuits using harvested AC voltage, but the RF frequency has to be orders of magnitude lower than the data path clock frequency. In addition, a dynamic memory cell was needed to preserve states between power supply cycles. Besides, substantial chip area was dedicated to power level detection and data-retention memory. He and Min [9] implemented all the digital building blocks of a Low Frequency (LF) RFID tag with adiabatic logic, while keeping a rectifier-based DC power supply for the remaining analog blocks. The intrinsic area overhead of adiabatic logic offsets the potential area saving obtained by partially eliminating the rectifier.

In this paper, we present the design of a passive RFID tag using RF-only logic, which permits digital operations to be performed from an AC power supply [10], as shown in Fig. 1(a). By eliminating the AC-DC rectifier and associated storage capacitors with little area overhead introduced, this approach will reduce the RFID chip area and cost. In addition, detailed solutions for minimum area design using RF-only logic and data preservation during the nulls in the ASK RF source are presented. This paper is organized as follows. In section II, we present RF-only logic and briefly discuss its structure and operation. Section III describes the system architecture. Section IV presents the circuit design of key building blocks. Results and discussions are shown in section V, and section VI concludes this work.

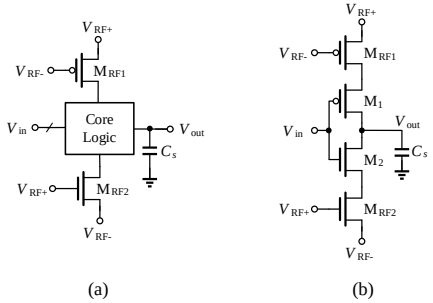

Fig. 1 (a) Generic RF-only logic structure with differential supply signals annotated. (b) Schematic of an RF-only inverter implemented in conventional CMOS

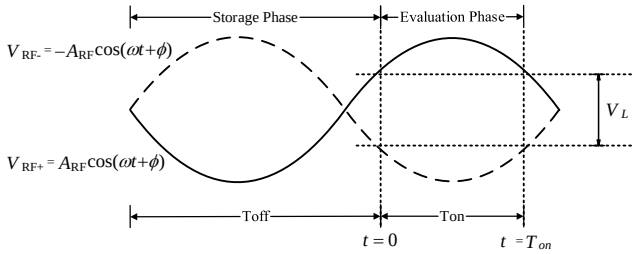

Fig. 2 Differential supply signals for RF-only logic with operation regions indicated

II. RF-ONLY CIRCUIT

The RF-only logic is a dual rail, AC powered logic concept as shown in Fig. 1(a). The structure of an RF-only logic can be divided into two parts: the logic evaluation part ("Core Logic") and a set of power supply transistors ("PST") M_{RF1} and M_{RF2} [10]. Core logic can be implemented with various logic styles, and we focus on conventional CMOS topology in this work. Fig. 1(b) shows the schematic of an RF-only inverter implemented with conventional CMOS. Operation is briefly explained as follows. During the evaluation phase the supply transistors are on and the core logic operates as normal. Outside this phase the supply transistors are off and the analog voltage is stored on the capacitor C_s. From a system perspective, the PST cells form a distributed power rectifying structure, which can be custom designed to meet local powering requirements. The output capacitance C_s represents the sum of the parasitic capacitance on the output node, and stores the charge on the output node to retain the voltage level while the power is off. The power supply RF frequency can be orders of magnitude higher than the supported clock speed in the data path.

III. SYSTEM DESIGN CONSIDERATIONS

Fig. 3 illustrates the system block diagram of the proposed rectifier-free UHF Gen-2 compatible RFID tag. It integrates a simplified power management unit, a RF front-end, a RO-based local clock source and the digital baseband. The induced differential RF voltages are clamped by the AC limiter to generate stable differential RF supply signals, which are used to power the rest of the chip. The powering and communication schemes are discussed in the following sections for a Gen-2 compatible design.

A. ASK compatible Powering Scheme

A Gen-2 compatible interrogator sends information to a tag by modulating a RF carrier using ASK. A tag receives the operating energy from this same modulated RF carrier [11]. The DC power supply in conventional RFID tag is constant during the entire inventory round, including low RF envelope periods. With RF-only based implementation, however, the RFID tag loses power during low RF envelope periods required by ASK signalling and has to be turned off, as shown in Fig. 4.

The powering scheme to manage this interruption is as follows. The state information in digital baseband is preserved in the custom-designed data-retention flip-flops for up to 12.5 µs, which is the maximum low RF envelope period according to the Gen-2 protocol. A RF-only based power level detection circuit monitors the RF envelope level transitions. In the case of a high-to-low level transition, the local clock signal is set to high, which prevents the state value in data-retention flip-flops from being contaminated by any unintentional latching during the transition periods. In the case of a low-to-high level transition, the local clock will not be activated until the state

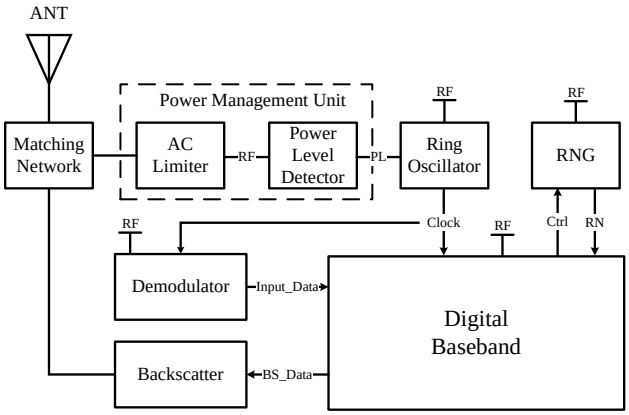

Fig. 3 System block diagram of proposed Gen-2 compatible RFID tag

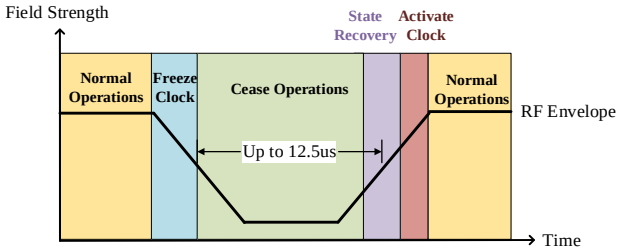

Fig. 4 RF envelope of Gen-2 forward link ASK modulation with powering scheme annotated

values in data-retention flip-flops are restored, and propagate through all the corresponding combination logics. Digital baseband logic operates as if there are no RF envelope low periods. A power-on-reset circuit is implemented to reset all the flip-flops upon initial interrogator power-up. The circuit level operation of the data retention flip-flop is explained in section IV.A.

Since the RF-only logic operates with an AC power supply, the bulk terminals of MOS devices cannot be tied to the RF sources directly to avoid forward-biased PN junctions. Two DC biasing voltages are generated from the RF source using a peak detection circuit to properly bias the bulk terminals of MOS devices.

B. Communication Scheme

Without a DC power supply, the conventional envelope detecting technique cannot be implemented for forward link ASK demodulation. However, the pulse-interval encoding (PIE) scheme used in Gen-2 forward link communication indicates that the useful information is only encoded in the length of the high RF envelope periods, as illustrated in Fig. 5. Therefore, a fully digital approach that counts the length of each high RF envelope period is implemented for the forward link demodulation. The demodulation block consists of a FSM and several pulse interval counters that are driven by a local 4MHz clock. The low-to-high RF envelope transition is used as the triggering clock for FSM.

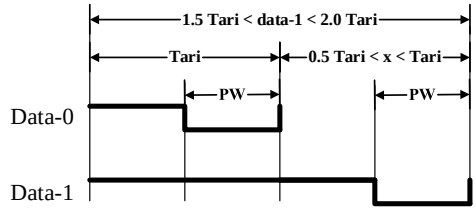

Fig. 5 PIE symbols for Gen-2 forward link [11]

A Gen-2 compatible RFID tag talks back to the interrogator by backscattering an unmodulated RF carrier: modulating the loading impedance of an antenna thus modulating the incident power. Phase modulation by changing the input capacitance of the RF front-end is implemented in this design since it maintains a constant RF amplitude for robust circuit operations.

C. Power Supply Transistor Sharing

To further reduce the area overhead introduced by the power supply transistors, a PST cell can be shared by a cluster of gates as depicted in Fig. 6. The gates that share one PST cell are selected such that no two gates can charge or discharge simultaneously [12]. These gates are called mutually exclusive gates and characterized separately. Thus, sharing of one PST cell amongst multiple logic cells will not degrade their performance. By implementing this algorithm on the digital baseband design, the number of PST cell is reduced by 56%.

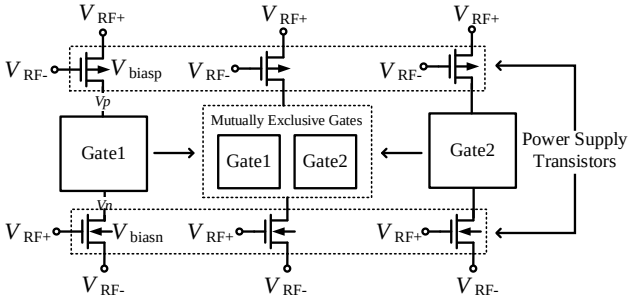

Fig. 6 Sharing power supply transistor among mutually exclusive gates

D. Digital Design Implementation

In UHF Gen-2 protocol, the RFID interrogator defines the forward link data rate. A 4MHz clock signal is generated locally on chip with a ring oscillator, and used as the global clock for digital baseband.

In order to implement the PST sharing scheme, core logic gates and PST cells are treated as separate standard cells, and PST cells are inserted after the generation of a gate level netlist. The layout of the PST cell is designed in the same fashion as other logic gate cells, as shown in Fig. 7. During placement, both logic cells and PST cells are treated as base cells that are placed in the standard cell arrays.

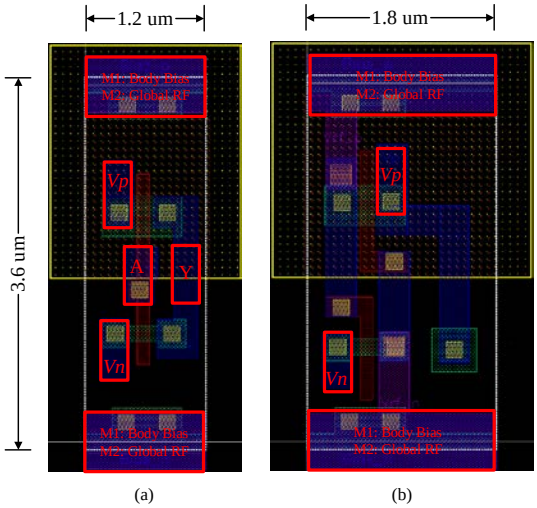

Fig. 7 Standard cell layout (a) RF-only inverter (b) PST cell

The four global nets: RF power nets V_{RF+}, V_{RF-} and body contact nets V_{biasp}, V_{biasn} are located on top and bottom of each standard cell, routed with M2 and M1, respectively. The local virtual power supply V_p and V_n as shown in Fig. 7, are routed as normal signal nets.

IV. KEY BUILDING CIRCUITS

A. Data-Retention Flip-Flops

The schematic of the proposed data-retention flip-flop is presented in Fig. 8. It is a master-slave type flip flop in differential configuration to enhance the driving strength. The master latch unit consists of clock controlled feedback inverters. And the slave latch utilizes stacked transmission gates to reduce leakage during low RF envelope periods. Similarly, the storage circuit is designed in differential 2-T DRAM configuration to enhance driving strength and reduce leakage. The storage circuit is driving a sense amplifier, which is comprised of cross-coupled inverters to sense the voltage difference of the stored charges and resolve to a logic level at the output during the power recovery phase.

There are four operation modes of the flip-flop that correspond to four phases of the RF envelope level, as illustrated in Fig. 9. The flip-flop operates only as a conventional rising edge triggered flip-flop when the RF envelope is high and stable, which corresponds to phase I. In phase II when there is a high-to-low RF envelope level transition, the clock input is kept at logic high to prevent any undesirable latching of an input signal. And the previously latched logic value is stored at the gates of M_1 to M_4 during phase III when the RF envelope level is low.

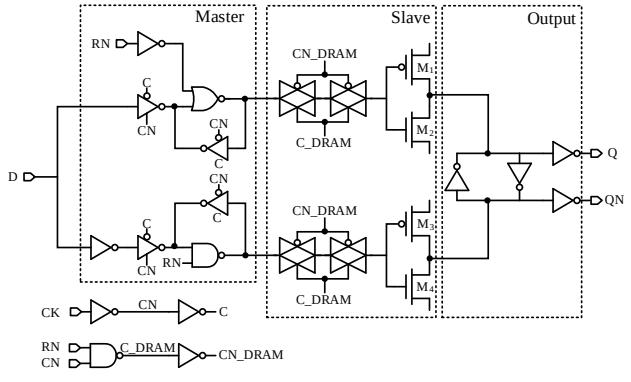

Fig. 8 Schematic of RF-only data-retention flip-flop

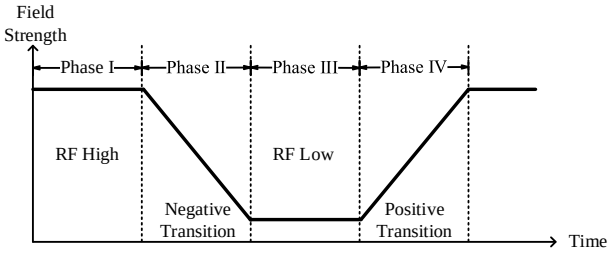

Fig. 9 Four phases of operation for the RF-only data-retention flip-flop

In phase IV when there is a low-to-high RF envelope level transition, the stored logic value is recovered and resolved to a logic level by the sense amplifier. The clock input will be kept at logic high before the complete recovery of stored logic value.

B. Power Level Detector

A power level detection circuit is designed to detect the transitions of RF envelope level. It freezes the local clock to logic "high", and thus stops the digital operations when the voltage is below a certain level.

Fig. 10 and Fig. 11 show the schematic and simulated waveforms of the power level detector. Signal V_{env} tracks the RF envelope with a small time constant. Transistor M_1 and capacitor C_{large} behave as a peak detector with a much larger time constant. V_{env} and V_{ref} are compared by a cross-coupled inverter-based sense amplifier. The difference in voltage is then resolved to logic levels using a latch, which is clocked by a free-running on-chip oscillator at 33MHz.

The key specifications of the power level detector are response time $T_{response}$ and effective range. The effective range is wide enough to cover the 1 µs – 8 µs range defined in UHF Gen-2 protocol. The corresponding normalized response time for transition time ranging from 0.5 µs to 8 µs is shown in Fig. 12.

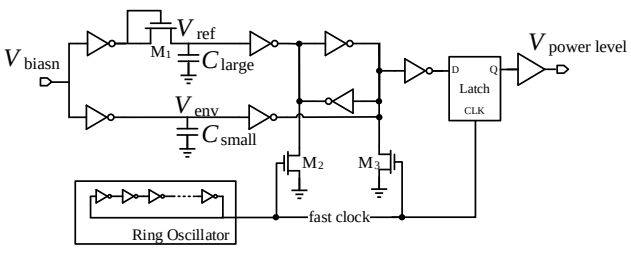

Fig. 10 Schematic of the power level detector circuit

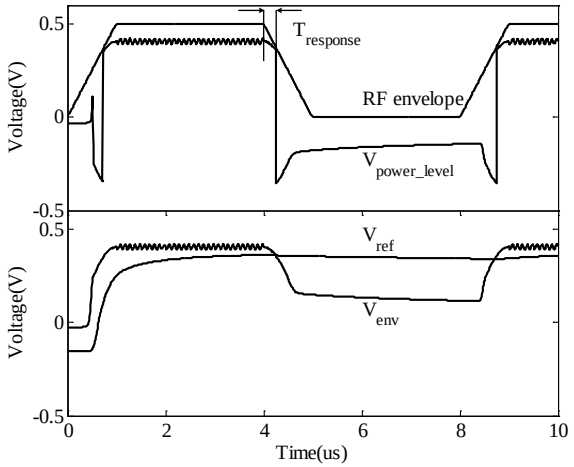

Fig. 11 Simulated signal outputs of power level detector

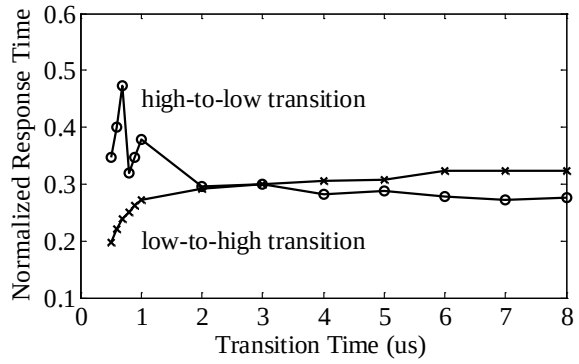

Fig. 12 Response time of power level detector

C. Backscatter Circuits

A reactive backscatter circuit is implemented as shown in Fig. 13. Two vertical natural capacitors $C_{bs1}$and C_{bs2} are connected in serial and controlled by two large switching transistors M_1 and M_2. The load reactance is modulated by M_1 and M_2 respectively.

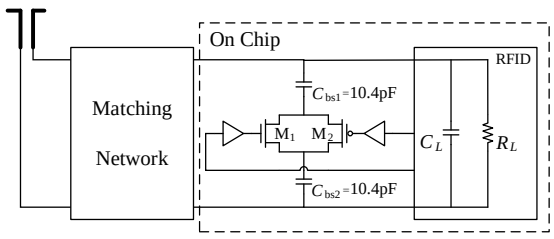

Fig. 13 Schematic of backscatter circuits

V. RESULTS AND DISCUSSIONS

This proposed rectifier-free UHF Gen-2 compatible RFID tag features a dimension of 0.6 mm × 0.3 mm as implemented in 0.13 µm CMOS technology. The simulated sensitivity at an induced RF amplitude of 500mV is 0dBm for the entire design. Table 1 summarizes the performance of this work compared to state-of-the-art designs.

TABLE 1

PERFORMANCE SUMMARY AND COMPARISON WITH OTHER UHF GEN-2 RFID TAGS

Chip	**This Work**	[6]	[2]	[13]
Technology	0.13µm	0.18µm	0.13µm	0.13µm
Tag area(mm^2)	0.18	1.1	0.55	0.95
Frequency range	860MHz-960MHz	860MHz-960MHz	860MHz-960MHz	13.56MHz, 860MHz to 2.45GHz
Supported standard	Gen-2	Gen-2	Gen-2	Gen-2
Sensitivity	0dBm	-0.4dBm	-14dBm	-10.3dBm

There are two limitations of the RF-only based rectifier-free design. The first limitation is the inability to generate a high voltage to program a conventional non-volatile memory. One solution to this limitation would be to employ RRAM technology.

The second limitation is the tradeoff between tag area and sensitivity. The low sensitivity of this implementation stems from the high static power dissipation of RF-only logic at high RF amplitude. This work is implemented with A_{RF} = 500mV, of which the power consumption is dominated by static rather than dynamic components. The system and circuit level solutions discussed in this paper apply for an implementation targeted at a lower RF amplitude. Gadfort [10] has demonstrated that single gate of RF-only logic can operate at RF amplitude down to 120mV. Since static power dissipation of RF-only logic decreases in cubical with respective to RF amplitude, a design of lower RF amplitude will largely reduce power consumption and improve tag sensitivity. However, an implementation with lower RF amplitude indicates larger gates to mitigate process variation and compensate for the reduced driving strength. The primary modification for a lower RF amplitude design involves characterizing the timing of standard cells and designing of the RF front-end for the targeted RF amplitude.

VI. Conclusion

We have presented a rectifier-free RFID tag design for cost reduction by using RF-only logic. A UHF Gen-2 compatible RFID tag has been developed in a 0.13µm CMOS process. For realizing the system, novel powering and communication schemes have been implemented. To further reduce area overhead, power supply transistors are shared among mutually exclusive gates without sacrificing performance. A standard cell library is designed and characterized for RFID application, including data-retention flip-flops. The overall RFID design features an area of 0.18 mm^2 and 0 dBm sensitivity at RF amplitude of 500mV in the simulation. The methodology discussed in this paper also applies for implementations of lower RF amplitude that trade off area for sensitivity.

VII. Acknowledgment

This work is funded by NCSU Chancellor's Innovation Fund and NSF.

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