Characterization of the Mechanical Stress Impact on Device Electrical Performance in the CMOS and III-V HEMT/HBT Heterogeneous Integration Environment

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Abstract— The stress impact of the CMOS and III-V heterogeneous integration environment on device electrical performance is being characterized. Measurements from a partial heterogeneous integration fabrication run will be presented to provide insight into how the backside source vias, alternatively referred to as through-silicon-carbide vias (TSCVs), used within the heterogeneous integration environment impacts GaN HEMT device-level DC performance.

Keywords— backside source via; GaN HEMT; heterogeneous integration; mechanical-stress-induced performance degradation; reliability; through-silicon-carbide via (TSCV).

I. Introduction

The heterogeneous integration of CMOS and III-V HBT and HEMT technologies seeks to dramatically improve designer flexibility by combining in a single chip stack various high-performance technologies. Within the heterogeneous integration paradigm, designers can choose the best technology for a particular task, and the integration of the various technologies is not limited in performance by off-chip connections prone to parasitic loading and other nonidealities. While the heterogeneous integration philosophy is setting the stage to offer designers many benefits, certain nonidealities exist which need to be understood to ensure a robust and reliable design. The thermal impact of integrating several distinct technology types certainly needs to be fully understood to capture temperature-dependent performance degradation and to identify mitigation strategies. Another unknown and potential limitation for heterogeneous integration is the mechanical stress impact of the integration environment on device electrical performance.

The purpose of this work is to characterize the impact of mechanical stress inherent to the CMOS and III-V heterogeneous integration environment on device electrical performance. Currently, work on two major fronts is underway. First, we seek to characterize the impact on device electrical performance due to various stressors present in the heterogeneous integration environment by means of a test chip which is shown in Figure 1. Secondly, we are virtually fabricating the CMOS and III-V device technology stacks using finite element (FE) simulation techniques to reveal the underlying stress distributions which cause device electrical performance shifts. Our long-term goal is to develop position-dependent transistor models which take into account the various stressors present in the heterogeneous integration environment such that designers can accurately observe circuit block performance prior to fabrication and make any necessary adjustments to the design. To produce the position-dependent models, we will incorporate the electrical measurement data obtained from our test chip and displacement fields obtained from FE simulation runs as shown in Figure 2. Models will be developed with the aid of third-party tools, in-house tools, or a combination of both.

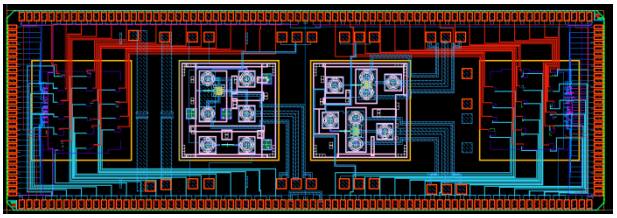

Fig. 1. Heterogeneous integration test chip with 65 nm CMOS chip and GaN HEMT, InP HBT chiplets.

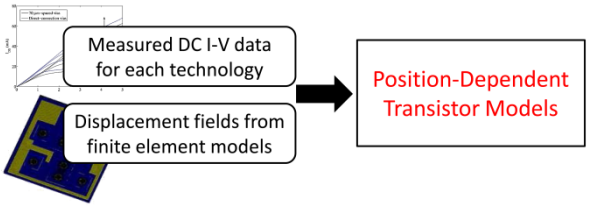

Fig. 2. Proposed workflow for obtaining position-dependent transistor models.

While the impact of mechanical stress inherent to the heterogeneous integration environment is relatively new and unknown, the impact of mechanical stress on device performance in other application spaces has been discussed

This work was supported by the Defense Advanced Research Project Agency (DARPA) DAHI Program under ARL contract number W911NF-13-1-0076.

previously: for example, mechanical stress impact of the silicon nitride (SiN) passivation step on GaN HEMT device performance [1], through-silicon via (TSV) impact on CMOS device performance in 3DIC stacks [2], and mechanical stress experiments to ascertain the performance impact on silicon germanium (SiGe) HBT devices [3]. The benefit of understanding the mechanical stress impact on device electrical performance is that it allows integrated circuit designers to better predict the actual performance of their circuits prior to fabrication, resulting in fabricated circuits with relatively high reliability. As such, we seek to extend this reliability prediction benefit to the CMOS and III-V HEMT/HBT heterogeneous integration space.

II. METHODOLOGY

By utilizing a fabrication run sponsored by our efforts on the DARPA DAHI project, a test chip (shown in Figure 1) was designed containing a 2 mm × 6 mm 65 nm CMOS chip with four 1 mm × 1 mm "chiplets," two each of GaN HEMT and InP HBT technology types.

Each technology has a specific mechanical stress mechanism that we seek to electrically characterize. For GaN HEMT devices, we seek to characterize the device-level electrical impact stemming from the use of backside source vias, alternatively referred to as through-silicon-carbide vias (TSCVs). For CMOS and InP HBT devices, we seek to characterize the impact of "microbumps," alternatively referred to as heterogeneous interconnects (HICs), on device electrical performance. We expect that the TSCVs will have a similar impact on GaN HEMT performance as through-silicon-vias (TSVs) do for CMOS devices. For CMOS and InP HBT devices, we are especially interested in characterizing the impact of contact deformation [4] that the HICs exhibit on these device types

As a partially fabricated version of our test chip shown in Figure 1 has been delivered to us containing the GaN HEMT devices, we focus the remainder of this paper on our GaN HEMT electrical characterization results. The CMOS portion of the chip is available as well; however, as the InP HBT chiplets are not available, there are no stressors for the CMOS available on the delivered chips (the InP chiplets provide the HIC stress for the 65 nm CMOS devices).

GaN HEMT Test Structures: The GaN HEMT test structures were fabricated in the Northrop Grumman Aerospace Systems (NGAS) GaN20 process [5]. Each test chip contains three four-finger GaN HEMT devices with 120 µm total gate width each in various configurations, shown in Figure 3, with respect to TSCV placement: i) TSCVs directly connected to the device source, ii) TSCVs spaced at a distance of 70 µm from the source, and iii) TSCVs offset from the device (we refer to this third test structure as the "baseline" variant for convenience). In Figure 4 we show cross-sectional views of simplified 3D models which provide details on TSCV placement for the direct-connection and 70 µm-spaced via GaN HEMT test structure variants.

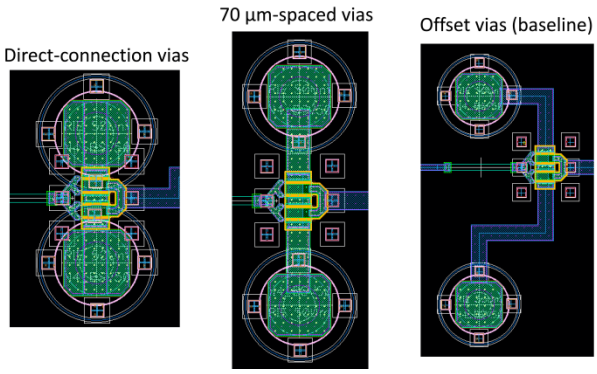

Fig. 3. Layout captures of the three GaN HEMT test structure variants.

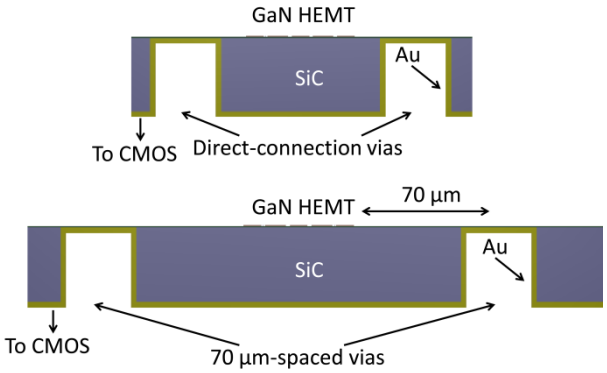

Fig. 4. Cross-sectional views of the simplified 3D models of the GaN HEMT test structures (baseline not shown).

III. EXPERIMENTAL RESULTS

As mentioned in [6], mechanical stress can impact the drain current of GaN HEMT devices. As such, the three GaN HEMT device variants shown in Figure 3 and associated pads were laid out to facilitate DC I-V characterization. As of this writing, nine test chips (each containing the three GaN HEMT variants) have been electrically characterized. We measured drain currents for the three device variants on a first chip and a second chip, respectively. The direct-connection via device yields the highest current and the baseline device has the lowest current, suggesting that the mechanical stress induced by the TSCVs has a noticeable impact on GaN HEMT drain current.

We measured the mean relative increase of the direct-connection device and the 70 µm-spacing via device over the baseline and found approximately a 6% increase.

As mentioned in [7], the gate current of GaN HEMT devices is also subject to variation in the presence of mechanical stress. As such, we compared the relative change in gate current for the three device variants, and show the compiled results in Figure 7. As before, dashed lines in the figure show linear approximations to the measured data. As shown in the figure, the direct-connection via device exhibits a larger increase in gate current magnitude relative to both the 70 µm-spacing device and the baseline device types. Thus, with the results shown in Figure 7, we again conclude that the TSCVs cause a noticeable, position-dependent change in GaN HEMT device electrical behavior.

IV. Stress Simulations

Finite Element (FE) modeling has been completed on one of the GaN chips. This modeling involves gridding the chip and running a process simulation so as to arrive at the final structure that is under stress due to the materials used, their differing Coefficients of Thermal Expansion (CTE) and the temperature steps in the processing.

Figure 5 shows the predicted distortion of this GaN chiplet before attachment to the CMOS, as obtained from the FE simulation. It has good general agreement with the measured distortion, obtained using a white light interferometry measurement (Figure 6).

Figure 7 shows the predicted stress map of this GaN chiplet, as obtained from the FE simulation. Of particularly interest is the stress impact of the TSCVs. Figure 8 shows the stress field around the vias as extracted from the stress map shown in Figure 7. This can be used to arrive at a keepout rule.

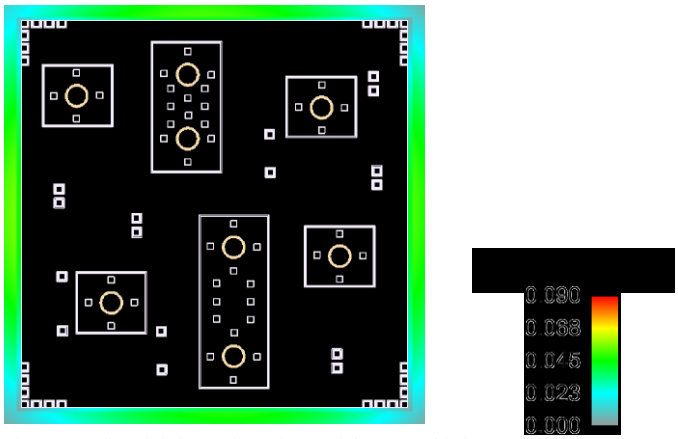

Fig. 5. Predicted deformation of one of the GaN chiplets.

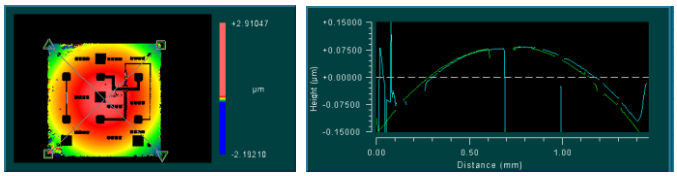

Fig. 6. Measured distortion of the same GaN chiplet.

V. Producing Postion Dependent Transistor Models

In addition to collecting DC I-V characterization data for the CMOS and InP HBT devices once they become available, the next step in this experiment will be to produce position-dependent transistor models for the GaN HEMT, InP HBT, and 65 nm CMOS technologies. The process by which the models will be developed is conceptualized in Figure 2, and may be accomplished with the use of third-party software tools, in-house tools, or a combination of both. A methodology for producing position-dependent CMOS models is described in [4], and the process developed in [4] may serve as a useful starting point for our efforts on this front.

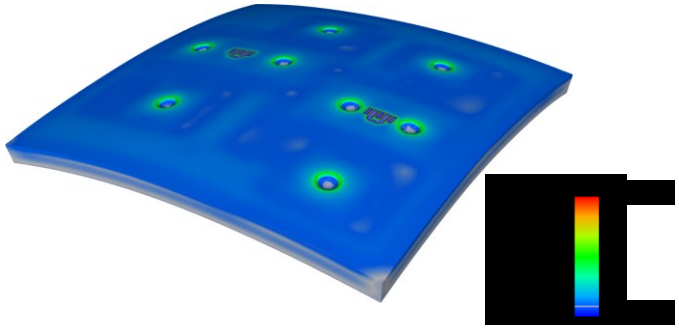

Fig. 7. Simulated maximum principal stress.

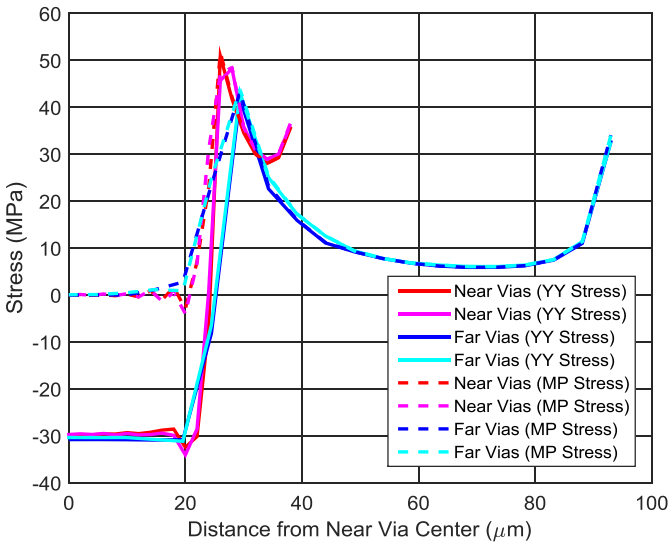

Fig. 8. Simulated stress in the vicinity of the TSCVs.

VI. Conclusion

In this paper we have presented our preliminary findings on the mechanical stress impact on electrical behavior in heterogeneously-integrated chip stacks. Our first set of measured results confirm that the TSCVs used to electrically connect the GaN HEMT devices to other heterogeneously-integrated blocks do indeed cause a measureable change in device behavior. We have also presented our general workflow which will be utilized to eventually produce position-dependent transistor models for design performance and reliability validation purposes in the heterogeneous integration design space.

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