Abstract:
This paper reports of a method for design of Extreme Environment (EE) electronics using the MOSFET body bias as a temperature compensation method. A Quadrature 435 MHz Voltage Controlled Oscillator (VCO) was used as the test element for design, modeling, and simulation. The VCO was simulated in an EE temperature environment between -250°C to +200°C and designed in the Honeywell 0.35 CMOS Partially Depleted Silicon On Insulator (PDSOI) technology. The VCO was optimized for EE by tuning the fourth device (body) terminal at selected devices. This paper also describes how a suitable Spice model was obtained.

Additionally, low power techniques are discussed for EE. Adaptive body biasing is used for optimizing the leakage of EE and adaptive supply voltage scaling was investigated to reduce the overall power.

Keywords: Extreme Environment; Temperature Invariant; Adaptive Body Biasing; Extreme Temperature; Adaptive Supply Voltage Scaling; Modeling; Bias Currents; Body Terminal

Introduction:
Previous lunar/planetary rovers used complex wiring harnesses to connect sensors to processing elements in a central artificial environment inside the rover that could be temperature controlled. It is anticipated that future vehicles will require distributed electronic architectures which will make temperature control more difficult [1]. In order to distribute these circuits outside this controlled environment, they need to be EE hardened for a minimum temperature range of -230°C (lunar pole), to +130°C (lunar day), to reach our nearest neighbor the moon. New circuit models for such ranges need to be developed. These techniques will help move towards distributed EE electronics that will reduce the size, complexity, and cost.

Wide temperature operation was achieved by using the body node of a transistor (Figure 1) as a 4th terminal that can be used to adjust device characteristics to compensate for temperature variations. The body terminal is readily accessible in PDSOI processes for each and every transistor, at some area penalty. It is also accessible in triple-well bulk CMOS processes, though at a larger area penalty.

A VCO was tuned for EE operation using the body node—the 4th transistor terminal shown in Figure 1—and a voltage source to apply a DC “correction” bias which negates extreme temperature effects.

Figure 1: Typical MOSFET device with 4th terminal
This paper is structured as follows: First, the temperature dependence of MOSFETs and their compensation is discussed. Second, the wide-temperature FET modeling approach is presented. Finally, the application of these techniques to the design of a Phase Locked Loop (PLL) is presented, before finishing with discussion of potential future work.

Initial Observations – Device Models:
It can be seen that the MOSFET saturation current
\[ I_{ds} = \frac{W}{L} \mu(t) \frac{Cox}{2} \left( V_{gs} - V_t(t) \right)^2 \]
has a temperature dependence that is a function of the mobility, \( \mu(t) \), and threshold voltage \( V_t(t) \) [3]. This results in temperature effects in operation of analog circuitry. At higher currents mobility \( \mu(t) \) has the dominant effect on \( I_{ds} \). The change in electron and hole mobility with temperature is shown in Figure 2 and Figure 3.

Figure 2: Electron Mobility vs. Temperature [3]. Reproduced with permission of author.
Modeling:
The provided Spice models supplied for the Honeywell 0.35µm process used in this study had not been characterized across a wide temperature range. Proper operation outside of the temperature range of commercial models required that we create new models which were valid for wide temperature ranges. It is a labor-intensive process to create a transistor model from experimental data. Ideally the models would have been created using specific test structures. However, to test our insight we had to use previously fabricated devices that were not designed with the required dimensions for creating a model. The commercial models had good correlation from 25°C to 200°C. Therefore, the BSIM3v3 model was numerically tuned to fit the measured data from -158°C to 25°C.

First, data was collected from the low temperature probe station at -158°C; which is the limit of our Variable Temperature Micro Probe System liquid nitrogen machine, Figure 4. The commercial models were simulated and then compared to the experimental data collected shown in (Figure 5). The models were then copied and turned into low temperature models by numerically tuning the temperature parameters until a closer fit was achieved; see (Figure 6). The standard models were off by 85% at -158°C while the numerically tuned models were off by 15% at -158°C. The models were then used to simulate a VCO that can operate from -250°C to 200°C.

Circuit Design:
Phase Locked Loops (PLL) are used in RF circuits for locking a receiver to a transmitter’s modulation signal. They are also used in digital circuits for clock synchronization. The block diagram of a Phase Locked Loop is shown in Figure 7. The most critical block is the Voltage Controlled Oscillator (VCO). The circuit schematic of the VCO is shown in Figure 8. This oscillator must be able to produce controlled oscillations over the full temperature range. We found that without compensation the VCO was only able to oscillate over a temperature range of -135°C to 200°C. We observed that outside this range the loop gain falls below unity, the point at which transistor M13’s current equals the loss conductance of the circuit. In other words, the VCO’s conductance is changing over temperature range; thus, M13 will demand more or less current than originally designed for. A VCO is an analog circuit whose operation requires a specifically designed current to work properly. It was interesting to observe that if the uncorrected models were used instead of the temperature corrected models, the simulation incorrectly predicted that the VCO would oscillate (though not function fully) over the entire temperature range!
At first, it was expected that all the NMOS and PMOS transistors would require compensation for the circuit to operate correctly over the temperature range. Through experimentation it was observed that this was not the case. Only the DC biasing transistor, M13, of the VCO needs to be corrected to achieve EE operation, as identified in Figure 8. The other transistors are not as sensitive to EE conditions because they are not operating in the saturation region. Vbody is used to compensate for the impact of temperature on the saturation current of M13. Figure 9 shows the body bias required to keep M13 supplying the proper bias current. The dotted red line shows the bias required for the standard commercial models; while the black line is the bias required from the corrected models.

To generate the DC body bias values for Figure 9 we used the criteria that the output amplitude of the VCO had to be no less than 100mV and the tuning range had to contain the 400 MHz to 500 MHz range shown in Figure 10. Using the standard commercial models (validated for -50°C to 125°C), which do not account for EE effects, the VCO works in the EE using body biasing; see Figure 11 and Figure 12. However, the VCO output signal is malformed in Figure 11. When the EE model (-250°C to 25°C) is used for temperatures below room temperature these amplitude oscillations go away, Figure 13, and the current consumed decreases by ~1mA because there is no longer a large disagreement between measured results and the model.
VCO Simulation: -250°C, 500MHz

Future Work:
Now that our initial investigation yielded promising results, additional test structures have been built in anticipation that an EKV model [2] can be created shown in (Figure 14). These new test structures have been created in the 0.18µm IBM7MLRF. The IBM process is not PDSOI. However, IBM’s is a triple well process in which each transistor is located in its own n-well or p-well. Hence the individual bulk terminal of a transistor can be accessed to vary the threshold voltage. Both a hot and a cold chamber will be utilized in creating the temperature models.

Future for Lower Power:
The ultimate goal of the Extreme Environment models is to enable Extreme Environment mixed signal circuits, such as PLLs. Leakage and power are important design considerations for distributed electronic circuits because of their battery-powered operation. In addition to improving the dynamic performance of the circuit, adaptive body biasing also helps to lower the standby leakage current of digital components. At higher temperatures, the leakage increases drastically due to rise in the subthreshold current. In order to extend the battery lifetime, it is therefore essential to maintain the leakage current within acceptable limits. Since the subthreshold leakage is exponentially dependent on the threshold voltage, large reverse body bias voltage can be used to lower the leakage. However, junction band-to-band tunneling (BTBT) leakage increases with reverse bias. An optimum reverse bias voltage lies at a point where the sum of both the subthreshold and BTBT leakage is minimal. Figure 11 shows the reverse bias voltage for minimum standby leakage for an NMOS transistor at different temperatures [4].

Figure 13: EE Model VCO Simulation at -250°C through DC Body Bias Correction

Figure 14: EKV Test Structures fabricated in IBM 0.18 µm process

Figure 15: Adaptive body bias trend for lower standby leakage in 90n IBM 7ML process. (a) -40°C, (b) 25°C, and (c) 125°C

The total power dissipation of the circuit largely depends on the dynamic power consumption. The supply voltage can be adaptively scaled for power savings since the dynamic power has a quadratic dependence on the supply voltage [4]. Figure 16 shows that adaptive voltage scaling can be implemented using a DC/DC converter and a feedback control loop to adjust the supply voltage. Table 1 shows the power savings achieved at different temperatures.
using an adaptive supply for a chain of cascaded inverters, which replicates the critical path in a circuit.

**Figure 16:** Adaptive Supply Voltage block diagram

**Table 1:** Adaptive Supply Voltage Scaling 0.35µm Honeywell PDSOI

<table>
<thead>
<tr>
<th>Temp at 500MHz</th>
<th>Power (mW) With fixed supply voltage</th>
<th>Power (mW) With adaptive supply voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>-230°C</td>
<td>34.95</td>
<td>32.53</td>
</tr>
<tr>
<td>-150°C</td>
<td>31.77</td>
<td>26.84</td>
</tr>
<tr>
<td>27°C</td>
<td>31.5</td>
<td>26.79</td>
</tr>
<tr>
<td>180°C</td>
<td>32.97</td>
<td>27.02</td>
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**Conclusion:**
Through tuning the DC bias on the 4th terminal of the transistor we increase or decrease the threshold voltage which compensates for EE effects in both analog and digital devices. Using this technique, future models, and the discussed adaptive circuit techniques; we believe we are well on the way to building a family of mixed signal circuits for the Extreme Environment.

**References**