A Zero Power Consumption Multi-Capacitor Structure for Voltage Summing in High-Speed FFE

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Abstract—**A Multi-Capacitor (MultiCap) structure for voltage summing is proposed. This passive structure replaces the current-summing block of a transmitter FFE and has zero power consumption. This MultiCap structure enables a potential power saving of more than 90% when incorporated within an ACCI system, including a voltage-mode FFE transmitter with MultiCap and a low-swing latch receiver. A transceiver designed in 0.13 standard CMOS process is able to achieve a speed of 5Gbps across a 75cm long FR4 channel with a power consumption of only 8.5mW, 1.7 mW/Gbps, in simulation. The MultiCap inherits all advantages of the AC Coupling Interconnect (ACCI) technology [4], including a density of 200um pitch. The available value for each individual capacitor of the MultiCap is in the 100fF range, with negligible parasitics.**

I. INTRODUCTION

Capacitively coupled interconnect utilizes capacitors in series with a channel to de-emphasis the low frequency component of the signal and, when combined with a low-pass channel, generate a flat band-pass response to eliminate inter-symbol-interference (ISI). The most critical component, the coupling capacitor, functions as a passive equalizer (EQ), enabling high speed communication with a simple low-power circuit [1]. The size of the capacitor, however, needs to be carefully selected to match the channel. When the capacitor is too big, the system is ISI-limited; when it is too small, the system is swing-limited [1]. Therefore, the fixed sizes of the capacitor pads in traditional ACCI create constraints on the length of channels and significantly increase the difficulty of designing for the rest of the system, including package and PCB floorplan.

An easy way to mitigate the variation in channel length is to implement an active EQ in the system, such as FFE or DFE. Typically a FFE (FIR) is used at the transmitter for its flexibility and ease of design. However, a FFE transmitter, such as [2] or [3], normally consumes a significant amount of power. The root of this problem is the use of a current summing block. Not only does the current-mode logic (CML) or DAC consume a lot of power, but it also complicates circuit design. One major problem for current summing is the limited dynamic range due to the maximum amount of current allowed on the summing branch in order to maintain the correct voltage on the summing node and prevent the circuitry from going out of saturation. Implementation of a feed-back block to maintain the current level would cost even more power.
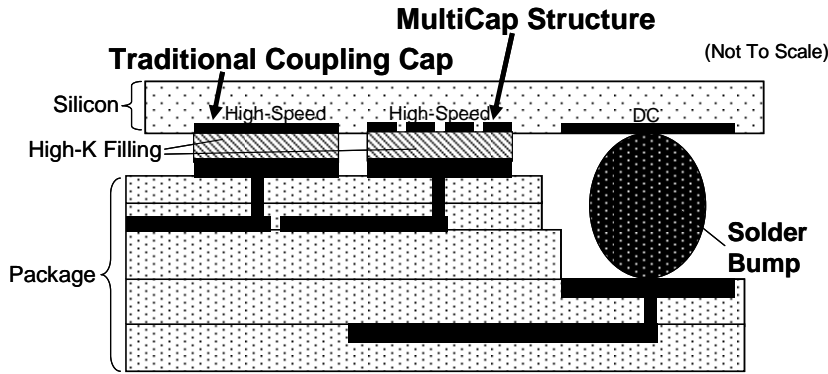

Fig. 1. The cross-section of an ACCI system with traditional coupling capacitor, *MultiCap*, and flip-chip bump
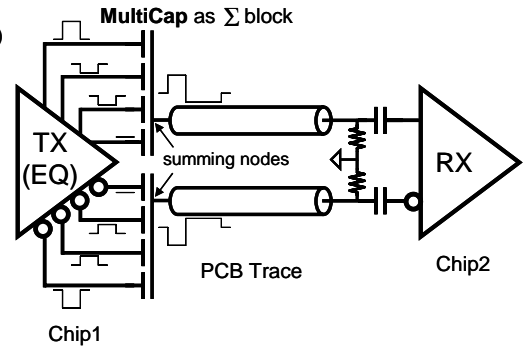

Fig. 2. A simplified schematic for a ACCI system with TX-side FFE where MultiCap is the summing block

A novel multi-capacitor (MultiCap) structure for the ACCI technology is proposed. This structure enables a simpler yet more efficient way to perform the summing function. Traditionally, the coupling capacitors in ACCI are formed by the top metal plates on the flipped chip and the package (left of Fig. 1). CMOS technology, however, has the advantage of much higher fabrication resolution than the package; therefore, it is straightforward to utilize this advantage toward creating the multi-capacitor (MultiCap) structure (center of Fig. 1) for signal coupling as well as voltage summing. The difference between the traditional coupling capacitor and the MultiCap structure is that the former has a single top plate, while the later has a matrix of discrete top metal plates. Each individual capacitor ($C_{C,i}$) of the MultiCap, as illustrated in Fig. 2, is connected to one branch of the FFE output driver, replacing both the voltage-to-current and current summing block. Instead of current being summed on a single branch, charges are summed on the shared bottom plate. Therefore, simple voltage-mode circuits can be used throughout the transmitter. The need for a steady tail current is eliminated and only dynamic power is consumed. Each branch of the FFE is independently coupled to one common bottom plate to solve the problem of a single dominant parasitic capacitor. Additionally, charges will be linearly summed at the bottom plate regardless of the magnitude of the voltage on the top plates. Similar concepts

can also be used on-chip whenever summing functions are needed, but this work is focused mostly on the application to ACCI technology.

This ACCI with MultiCap system is identical to traditional ACCI from the bottom plate in package to the receiver [1]. And it inherits the advantages of ACCI, including high I/O density, potential to improved yield, and increased long-term reliability [4].

II. ANALYSIS OF PROPOSED MULTI-CAPACITOR STRUCTURE

The top of the MultiCap Structure, Fig. 3, is an array of individual capacitances ($C_{C,i}$) to be connected to the FFE voltage-mode driver. The number of rows equals the number of taps of the FFE (N_{tap}), and the number of columns equals 2^R, where each tap has R-bit resolution. All $C_{C,i}$ are of identical geometries therefore, the tap weights of the FFE are set by whether each branch has a signal or not. It is important for each individual $C_{C,i}$ to be identical to keep the circuit design simple. The variables used in the following equations are the plate geometries (w, h, and s), plate area (A_{pad}, and A_{Cci}), dielectric constant (k), shown in Fig. 3. Note that the spacing (s) is neglected in most of the equations when calculating the MultiCap geometries.

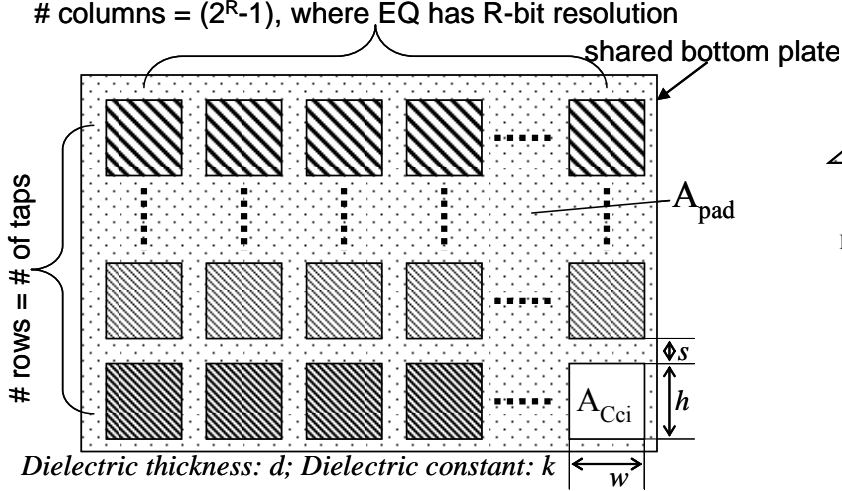Fig. 3. Top view of the MultiCap structure
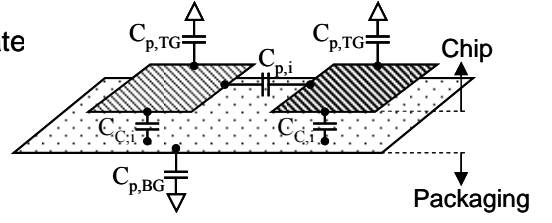

Fig. 4. The capacitances between a pair of $C_{C,i}$ and ground
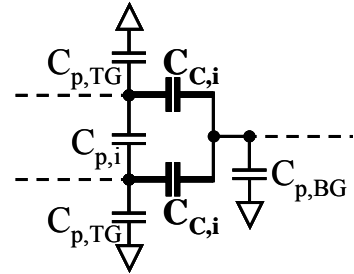
Fig. 5. Schematic model for the pair of $C_{C,i}$ shown in Fig. 4

A. Parameter Analysis of the MultiCap Structure

The values of $C_{C,i}$, like all parallel-plate capacitors, are determined by the size of the overlapping plate area (A_{Cci}), the dielectric thickness (d), and the dielectric constant (k):

$$C_{C,i} = k\varepsilon_0 \frac{A_{Cci}}{d} \tag{1}$$

The upper-bound of the area of each top plate, $A_{Cci,max}$, is limited so that the total area of the MultiCap is smaller than the bottom plate. Thus, (2) can be derived, where A_{pad} is the area of the bottom plate.

$$A_{Cci,max} = \frac{A_{pad}}{N_{tap} \times (2^R - 1)} \tag{2}$$

In special cases, $A_{Cci,max}$ may be more than shown in (2). For instance, the total number of top plates is no longer (2^R-1) when the FFE has different maximum tap weight for each tap. Nonetheless, $A_{Cci,max}$ can still be calculated by assuming each top plate is identical, and the following equations can be modified accordingly.

The minimum area of each top plate, $A_{Cci,min}$, is implicitly limited by the minimum receiver sensitivity. That is, the total capacitance of one row of the MultiCap, $C_{C,row,min}$, should be large enough such that the receiver is able to detect the non-equalized signal after attenuation over the longest channel. The value of $C_{C,row,min}$ should be estimated from a preliminary simulation, which includes an ideal driver and a ACCI channel, allowing the total equivalent area of the entire row of top plates, $A_{Cc,row,min}$, to be calculated:

$$C_{C,row,min} = k\varepsilon_0 \frac{A_{Cc,row,min}}{d} \Rightarrow A_{Cc,row,min} = \frac{d}{k\varepsilon_0} C_{C,row,min} \tag{3}$$

Thus, the corresponding minimum area of each top plate, $A_{Cci,min}$, can be derived:

$$A_{Cci,min} = \frac{A_{Cc,row,min}}{(2^R - 1)} = \frac{d}{k\varepsilon_0 (2^R - 1)} C_{C,row,min} \qquad (4)$$

A larger A_{Cci} is preferable because, unlike the non-EQ version where coupling capacitance is larger than necessary causing ISI [1], the EQ is capable of either tuning down the driving power for shorter channels or generating more high-frequency components for longer channels, thereby eliminating ISI.

From (2) and (4) the range of the MultiCap area is limited mainly by two variables, A_{pad} and $C_{C,row,min}$. The former is related to I/O density and the later to circuit capability. By substituting (2) and (4) into (1), then combining, results in (5) then (6).

$$\frac{C_{C,row,min}}{(2^R - 1)} \le C_{C,i} \le \frac{k\varepsilon_0 A_{pad}}{d \times N_{tap} \times (2^R - 1)} \qquad (5)$$

$$C_{C,row,min} \le \frac{k\varepsilon_0 A_{pad}}{d \times N_{tap}} \qquad (6)$$

Equation (6) shows the relationship between three of the most dominant variables for this ACCI system with MultiCap: the geometries (A_{pad} and d), the property of the dielectric filling (k), and the circuit complexity (N_{tap} and, implicitly, $C_{C,row,min}$). In order to satisfy (6), when driven toward higher-density I/O, the area of the bottom plate is then limited, thus a higher dielectric constant is needed. Alternatively, the same goal can be achieved by decreasing the dielectric thickness, decreasing the circuit complexity (N_{tap}), such as lower N_{tap}, or improving the receiver sensitivity, hence lowering $C_{C,row,min}$.

For example, given a set of variables; $A_{pad} = 175 \times 175 um^2$ (200um pitch and 25um spacing on package from [4]), $C_{C,row,min} = 500fF$ (from preliminary simulation with 75cm microstrip on FR4 and 0.13um standard CMOS for circuit), d = 1um (assumed), k = 18 (from [5]), $N_{tap} = 4$, and R = 3, substituting into (5) results in:

$$71.5\,fF = \frac{500 \times 10^{-15}}{(2^3 - 1)} \le C_{C,i} \le \frac{18 \times 8.85 \times 10^{-12} \times (175 \times 10^{-6})^2}{1 \times 10^{-6} \times 4 \times (2^3 - 1)} = 174.2\,fF \qquad (7)$$

If the high-k dielectric (k =18) used above is not available, and an ordinary oxide is used instead, (6) will not be satisfied unless the circuit complexity is decreased (N_{tap} or R), or the receiver sensitivity is increased.

B. Parasitic Capacitance

There are two types of parasitic capacitances in the MultiCap structure, shown in Fig. 4 and 5, vertical ($C_{p,TG}$, and $C_{p,BG}$, coupled to ground) and horizontal ($C_{p,i}$, coupled to next row of MultiCap). The vertical capacitances, $C_{p,TG}$ and $C_{p,BG}$, are between the top plate and the on-chip ground plane, and between the bottom plate and the package ground plane. They are treated as constants from manufacturing process, due to the fixed height between plates and ground planes, and can be minimized by placing a cutout in the ground plane where the MultiCap is located. The other significant parasitic component is the horizontal fringe capacitance, $C_{p,i}$, between two rows of the MultiCap. The ratio between $C_{p,i}$ and $C_{C,i}$ can derived:

$$\begin{cases} C_{C,i} = k\varepsilon_0 \dfrac{wh}{d} \\ C_{p,i} = k\varepsilon_0 \dfrac{wd}{s} \end{cases} \Rightarrow R = \frac{C_{p,i}}{C_{C,i}} = \frac{d^2}{sh} \qquad (8)$$

The ratio's dependency on w is eliminated in (8) because of the one shared width. The parasitic capacitance between columns can be calculated in the same manner (with eliminated h) but is ignored due to both terminals of the capacitor being connected to the same tap of FFE. Also, the ratio is independent of k only if the dielectric filling is homogeneous (the dielectric filling is patterned), or the chip top metal is buried under oxide. Under normal circumstances, when d ≈ s, the ratio is about d/h. If h>>d, $C_{p,i}$ is negligible.

Figure 6 shows a comparison between calculated results using (8) and EM simulation results using Sonnet Suites (EM and model extraction). It is shown from both curves that $C_{p,i}$ is less than 10% for a spacing larger than 1um. EM simulation shows more parasitic capacitance because it takes into account the fringe capacitance.
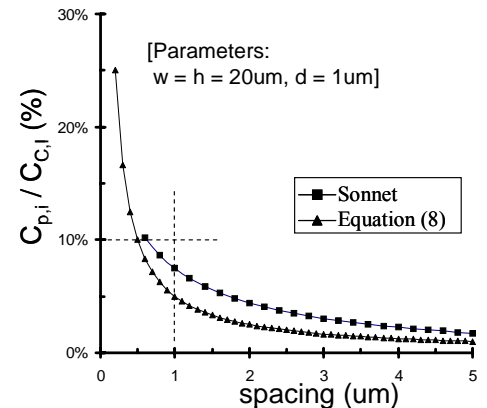

Fig. 6. Calculation results using (8) vs. Sonnet simulation result

III. IMPLEMENTATION OF MULTICAP AND TRANSCEIVER

ACCI technology utilizes small coupling capacitors for low-swing pulse signaling [1], in contrast to non-return-to-zero (NRZ) signaling used in typical high-speed chip-to-chip interconnect [2]. The relationship between the size of the coupling capacitor and signaling method is presented in [6]. For the MultiCap structure implemented in this work, the capacitance ($C_{C,row}$) is relatively small, and only pulse signaling is supported. MultiCap can also support NRZ if the capacitance is large enough ($C_{C,row}$ > 10pF preferably).

The FFE transmitter and the simple latch receiver circuit, adapted respectively from [7] and [8], are designed in standard 0.13 CMOS technology. A $C_{C,i}$ value of 150fF, calculate from (7) for the density of 200um pitch, is chosen for the MultiCap. The channel is a coupled microstrip on regular FR4 PCB with 5mil width and spacing and a length of 75cm (30 inches). Figures 7 and 8 show the simulated waveform of the receiver input before and after equalization is enabled. From the open eye (pulse signal) in Fig. 8, it is demonstrated that the transmitter FFE with MultiCap alone is capable to compensate for the low-pass response of the channel. Therefore, a simple receiver using a non-clocked differential latch following a gain stage can be used. When transferring a data stream at 5Gbps across a channel up to 75cm in length, the simulated power consumption is 7.2mW for the transmitter and 1.3mW for the receiver, yielding a power efficiency of 1.7mW/Gbps for the whole ACCI transceiver with MultiCap. If only FFE transmitters are compared, as shown in Table 1, the MultiCap FFE structure has a potential power saving of more than 90%.

Table 1. Comparison of FFE transmitter performances

	This Work	[2]	[3]
Process (um)	0.13	0.13	0.11
TX Power (mW)	7.2*	221	150
Speed (Gbps)	5	6.25	6.4
TX Power Efficiency (mW/Gbps)	1.44	35.3	23.4

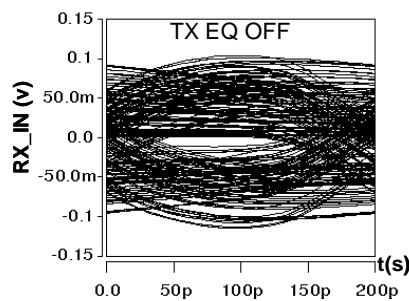* No serializer incorporated.

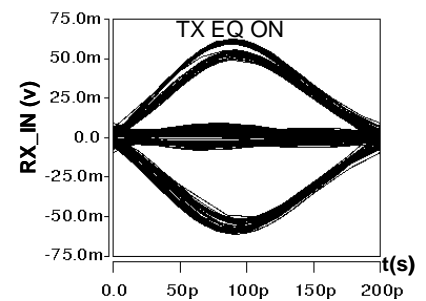Fig. 7. Eyediagram of the ACCI receiver input when the TX FFE is disabled

Fig. 8. Eyediagram (pulse signaling) of the ACCI receiver input when the TX FFE is enabled.

IV. CONCLUSION

A MultiCap structure compatible with ACCI technology is proposed. The parameters of the MultiCap can be calculated and selected from a set of equations. It is demonstrated that this structure is able to replace the summing block of a FFE transmitter. Combined with proper FFE design, the MultiCap enables high-speed low-power (1.7mW/Gbps) chip-to-chip communication with the flexibility of active equalization.

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