

Circuit/Channel Co-Design Methodology for Multimode Signaling

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Abstract

As higher density of interconnects and packages are demanded, crosstalk noise is becoming more important in input/output (I/O) design. The multimode signaling scheme offers effective crosstalk cancellation in high density links. This paper presents a new circuit/channel co-design methodology for high density links with multimode signaling. A detailed design approach is introduced and a detailed channel design optimization example is provided to validate this method. The optimized channel shows over 60% root mean square (RMS) jitter reduction compared with single-ended signaling. The printed circuit board (PCB) and package routing density of the optimized channel are 300% and 97% higher compared with a practical benchmark channel, respectively, and still shows 31% jitter reduction.

Introduction

As system performance advanced in recent years, higher density of interconnects, aggressive scaling of input/output (I/O) bandwidth and denser packages are in demand. However, high density chip-to-chip links tend to suffer from severe crosstalk noise. A crosstalk cancellation coding scheme referred to as multimode signaling offers the ability to improve wiring density but so far has been investigated mainly for uniform channels and channels with small discontinuities [1]–[4]. To make best use of crosstalk cancellation by multimode signaling in real world applications, practical channels including packages, sockets and printed circuit boards (PCBs) need to be considered. However, optimum implementation of a realistic multimode signaling sub-system requires a systematic approach to co-design the circuits and the interconnect channel. This paper describes a design methodology for multimode signaling circuit/channel co-design. A fully tunable multimode signaling transceiver is designed to implement the coder/decoder (CODEC). Both the CODEC coefficients and individual channel timing parameters are tunable. The methodology works as follows. First, the set of baseline CODEC coefficients and timing parameters are derived from the S-parameters [5] extracted from the baseline channel design. Then the different components in the channel are tuned for skew and impedance so as to minimize the root mean square (RMS) jitter and bit error rate. Thus the circuit and channel are co-optimized, with the goal of maximizing channel density. The detail optimization process is illustrated by an example channel which has PCB and package signal routing. The jitter reduction and eye height over traditional single ended signaling and multimode signaling are quantified for comparison. The optimized channel is compared to a practical benchmark channel [5] as well to show the signaling improvement for high density channels.

Design Methodology Overview

The design methodology consists of three major steps as shown in Fig. 1. First, we make parameterized models of PCB interconnect and package. In order to achieve the maximum density, we construct the baseline channel with the minimum trace width and spacing design rules. Then, S-parameters are extracted from each part of the full channel which is used to generate the CODEC for multimode signaling with a MATLAB routine. Once the CODEC is generated, it will be implemented in a fully programmable transceiver we designed to evaluate the channel and the CODEC. After evaluating the eye diagram, we determine whether we need larger spacing, wider trace or any other modifications to the channel. By repeating the above steps, we can maximize the channel density while having control over signal integrity.

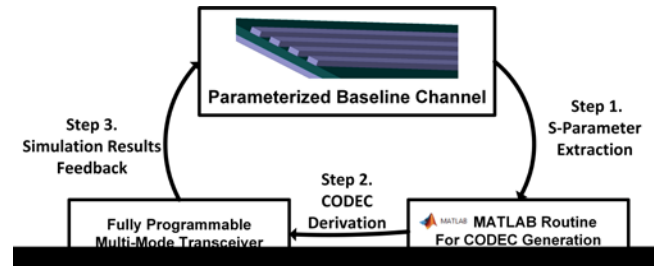


Figure 1. Design method illustration.

In this work, we consider an embedded microstrip bundle consisting of four lines as shown in Fig. 2 for both board routing and package routing with different size and spacing. For the PCB design, the thickness of solder mask, dielectric substrate, signal trace and reference plane are 10 μm , 70 μm , 50 μm , and 50 μm , respectively. The minimum signal trace width and spacing are both 100 μm . For package design, the thickness of solder mask, dielectric substrate, signal trace and reference plane are 20 μm , 25 μm , 15 μm , and 15 μm , respectively. The minimum signal trace width and spacing are both 15 μm . In short, our baseline model has signal trace width and spacing of 100 μm for the PCB and 15 μm for the package routing.

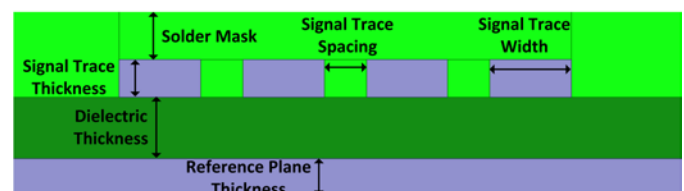


Figure 2. Cross-section of routing traces.

For a given length, the S-parameter matrix of the model can be extracted from a 2-D electromagnetic field solver such as the one in ANSYS Q3D Extractor.

A method that extracts the CODEC for multimode signaling from the S-parameters of a channel is available [5]. With the assumption of perfect termination and no reflections, a direct relationship between transmitted voltages and received voltages can be established as shown in (1):

$$V_{out} = S V_{in} \quad (1)$$

Here S is constructed from a subset of the S-parameters of the channel. Then with CODEC matrix T diagonalizing the S matrix, we have crosstalk noise minimized as shown in (2):

$$V_{out} = T^{-1} S T V_{in} \quad (2)$$

To easily implement the CODEC matrix in the multimode transceiver, we need the transceiver to be fully programmable which means that we do not have to redesign or retune the circuit for different channels. Since implementing the CODEC on the receiver side would require complex circuits, we use a circuit with only transmitter encoding [6] for programmability. The topology of the circuit is as shown in Fig. 3. We can see that two major parts are phase adjustments and main drivers. The delay chain generates 4 different phases of each binary signal; these 16 bit signals along with their inverse signals are sent into each CODEC driver. In the driver, we use the current summation scheme as shown in Fig. 4. The NMOS transistor gates at the bottom are connected to control bias signals, and the transistors at the top are connected to pre-delayed signals. By setting control bias signals we can choose which signals are in the summation equation for programmability. Because the transistor's current is proportional to its width, the magnitude of the CODEC can be controlled by weighting the width of the transistors. The sign of the CODEC is controlled by choosing whether to turn on the path of the signal or inverted signal. Thus, both magnitude and sign of the CODEC can be fully programmed and easily implemented.

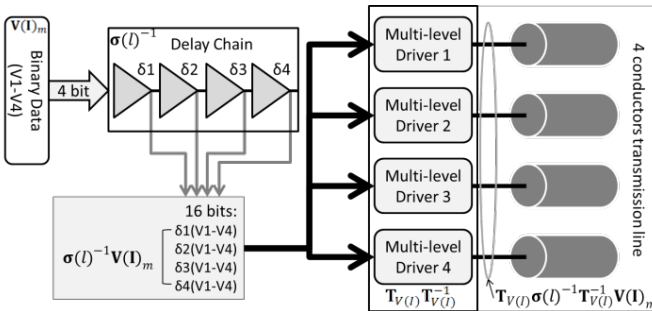


Figure 3. Block diagram of transmitter circuit.

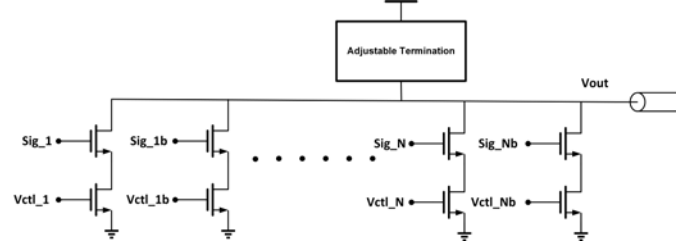


Figure 4. Schematic of the CODEC driver.

Example Channel Design

We begin the channel design with the PCB only baseline channel with minimum signal trace width and spacing of 100 μm . We target a signaling rate of 4 GT/s and a wiring length of 4.25 inches. To examine the coupling between the signal lines, we extract the RLGC matrix of the 2-D model as shown in Table. 1. We can see that the mutual capacitances and inductances are comparable to the self-capacitances and self-inductances, which is expected since the channel is highly coupled.

$L_o = 3\text{e-}07$	(H/m)			
$6.8\text{e-}08$	$2.9\text{e-}07$			
$2.4\text{e-}08$	$6.5\text{e-}08$	$2.9\text{e-}07$		
$1.4\text{e-}08$	$2.4\text{e-}08$	$6.8\text{e-}08$	$3\text{e-}07$	
$C_o = 10.8\text{e-}11$	(F/m)			
$-1.4\text{e-}11$	$11.3\text{e-}11$			
$-1.1\text{e-}12$	$-1.4\text{e-}11$	$11.3\text{e-}11$		
$-0.8\text{e-}12$	$-1.1\text{e-}12$	$-1.4\text{e-}11$	$10.8\text{e-}11$	
$R_o = 118$	(Ω/m)			
23	117			
11	22.3	118		
7.5	11	22.8	118	
$G_o = 0.05$	(S/m)			
-0.003	0.05			
$-1.9\text{e-}6$	-0.003	0.05		
$-5\text{e-}9$	$-1.8\text{e-}6$	-0.003	0.05	

Table 1. RLGC model of PCB only channel.

To further evaluate the coupling effect of this baseline channel, we examine the eye diagram with traditional single ended drivers without any coding in Fig. 5. As comparison, we would like to see the impact of inter-symbol interference (ISI) on the channel by exciting only one signal trace instead of four. Signals are transmitted at 4 GT/s. Comparing Fig. 5 and 6, we can see that with strong coupling, the jitter has increased from 23 ps to 70 ps due to crosstalk-induced jitter (CIJ). Thus, our goal here is to minimize the CIJ as much as possible with multimode signaling.

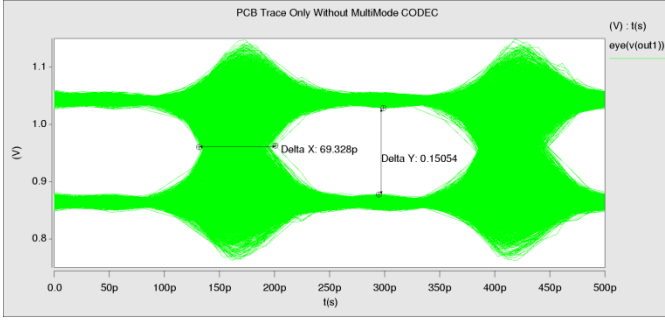


Figure 5. Eye diagram for PCB channel without CODEC.

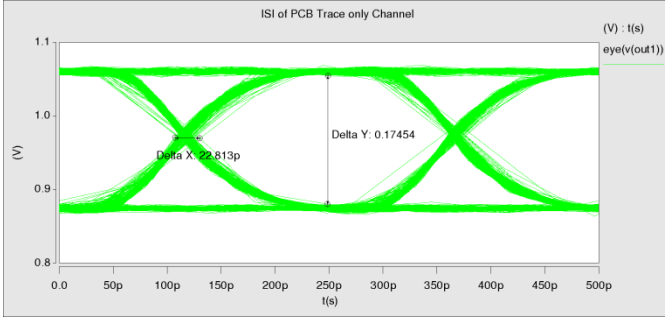


Figure 6. Eye diagram for ISI of PCB channel.

After time domain analysis of the baseline channel, we extract the S-parameter file with the ANSYS Q3D Extractor 2-D field solver to generate CODEC matrices T and T^{-1} for multimode signaling as shown in Table 2. The numbers in the CODEC matrices given are rounded approximations for implementation. To evaluate the frequency domain performance of the baseline channel and the effectiveness of the CODEC derived, we plot the original reduced S-parameter matrix S and the modified reduced S-parameter matrix $T^{-1}ST$ in dB. To make the plot concise, only two traces out of four are plotted here. The figure of merit is magnitude difference between diagonal entries and off-diagonal entries in dB. The good performance in crosstalk noise suppression is expected since we use a uniform channel without any discontinuities. Fig. 7 shows that the modified S-parameter entries have 16 dB crosstalk noise suppression compared to the original S-parameter entries at 4 GHz, and 17 dB at 10 GHz. This confirms that the generated CODEC provides a significant signal-to-noise ratio (SNR) improvement. This CODEC is implemented in the multimode transceiver to evaluate the jitter reduction performance in the next step.

$$T = \begin{bmatrix} 0.6 & -0.5 & 0.5 & -0.3 \\ 0.3 & -0.5 & -0.5 & 0.6 \\ -0.3 & -0.5 & -0.5 & -0.6 \\ -0.6 & -0.4 & 0.5 & 0.3 \end{bmatrix}$$

$$T^{-1} = \begin{bmatrix} 0.6 & 0.3 & -0.3 & -0.6 \\ -0.5 & -0.5 & -0.5 & -0.5 \\ 0.5 & -0.4 & -0.4 & 0.5 \\ -0.3 & 0.6 & -0.6 & 0.3 \end{bmatrix}$$

Table 2. Rounded CODEC matrices for PCB only channel.

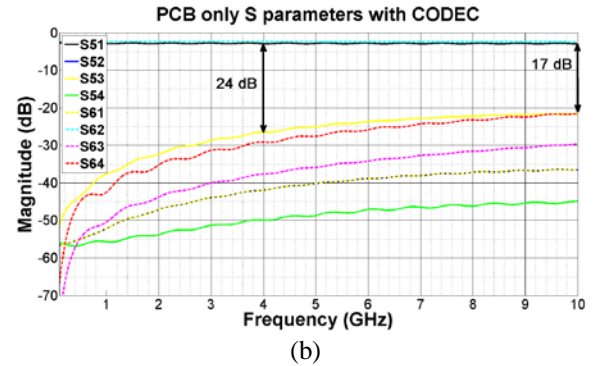
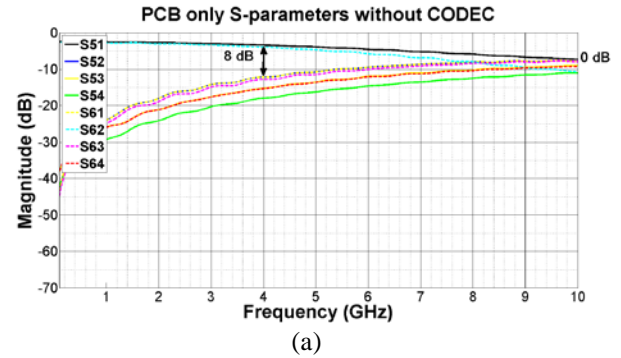


Figure 7. S-parameters for PCB only channel: (a) Original S-parameters and (b) modified S-parameters.

By setting the control signal sequence, we implement the CODEC in Table 2 in the transmitter circuit in Fig. 3. With the particular trace width selection, the characteristic impedance of the traces is around 50Ω . We set the termination resistance to be 50Ω at both ends of the channels, and assume 0.5 pF parasitic capacitive loading at both the transmitter and receiver for the simulation. By tuning the timing adjustments δ_1 – δ_4 to compensate the delay of each mode, we minimize jitter at the receiver side. Fig. 8 shows that while the eye height is about the same as for traditional single ended drivers, the RMS jitter is reduced from 69 ps to 26 ps, a 62% improvement. We can also see that this jitter value is very close to the ISI jitter value of 23 ps which does not have any crosstalk noise. Thus, we conclude that the minimum trace width and spacing might be used in a practical PCB channel with multimode signaling.

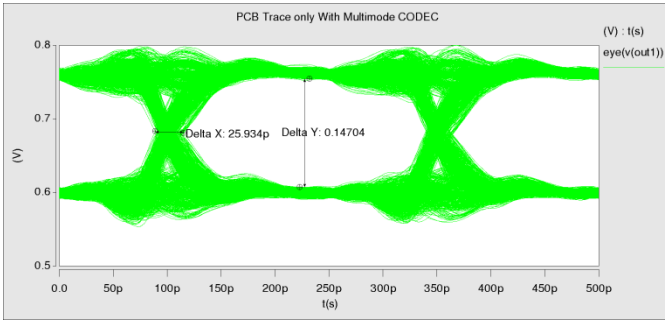


Figure 8. Eye diagram for PCB channel with multimode signaling.

Next, we will focus on the package design for the full channel. In this paper, we did not include any 3-D discontinuities such as via, plated through-hole (PTH), or socket for simplicity. We focus on the trace routing on package, and try to increase the routing density as much as possible. We assume microstrip for package routing similar to the PCB board as mentioned above. For the high routing density, we construct the baseline package with minimum trace width and spacing of $15\ \mu\text{m}$. Instead of examining the package itself, we consider the full channel scenario which is package plus PCB board channel plus another package. The length of package routing trace is set to be 2.5 cm, and the data rate is again 4 GT/s. Then, the S-parameters of the two packages are extracted and cascaded with the PCB channel for evaluation and generating the CODEC of the full channel.

With the minimum spacing and width design rules, the eye diagram for the traditional single ended signaling is shown in Fig. 9. The RMS jitter is 68 ps, roughly the same as for the PCB only case, but the eye height is considerably smaller at around 80 mV. Then, the same procedure as for the PCB only channel is repeated to examine this full channel. First, the S-parameters of the package model are extracted and cascaded with that of the PCB channel, then a CODEC is generated from the S-parameters of the cascaded full channel model. After that, by implementing the generated CODEC in the transceiver, the performance of multimode signaling with the full channel is examined. Fig. 10 shows that with multimode signaling the RMS jitter is reduced to 29 ps, a 57% reduction compared with single-ended signaling in Fig. 9 with an eye height of 62 mV.

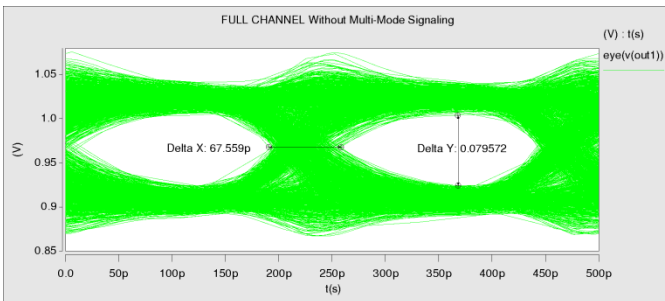


Figure 9. Full channel without multimode signaling.

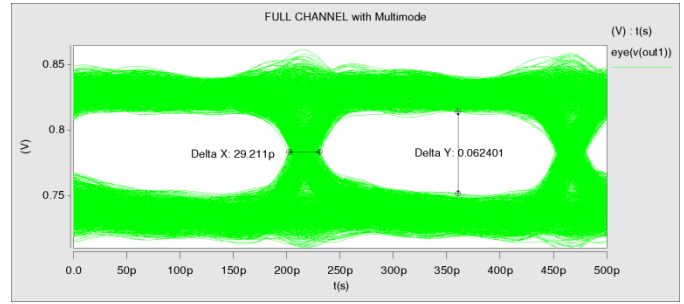


Figure 10. Full channel with multimode signaling.

We can see large floor noise in the simulations which causes the small eye height. Since we used the minimum design rules, it is speculated that there may be a characteristic impedance mismatch between the package and PCB which causes this problem. It turns out that the characteristic impedance of the package signal line is $67\ \Omega$ which is significantly higher than that of the PCB channel at $50\ \Omega$. By increasing the signal trace width to $34\ \mu\text{m}$ and keeping the spacing the same at $15\ \mu\text{m}$, we match the characteristic impedance to $50\ \Omega$. By going through the same procedure (S-parameter extraction, CODEC generation, and implementation in transceiver circuit) we generate the eye diagram to examine the new channel. Fig. 11 shows the matched channel with traditional single ended signaling. The floor noise is reduced with the matched impedance and the eye height is increased to 117 mV. The matched channel also improves multimode signaling as shown in Fig. 12, the RMS jitter is 26 ps compared with 29 ps for the minimum width case, and the eye height is 76 mV compared with 62 mV.

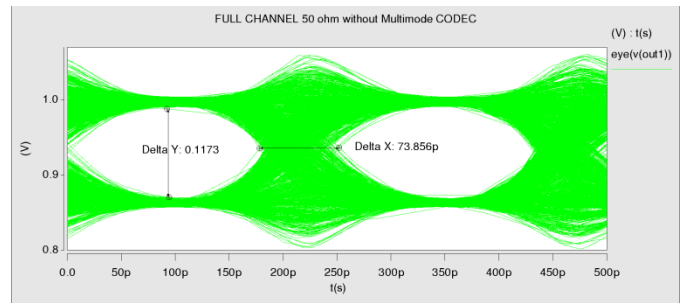


Figure 11. Full matched channel without multimode signaling.

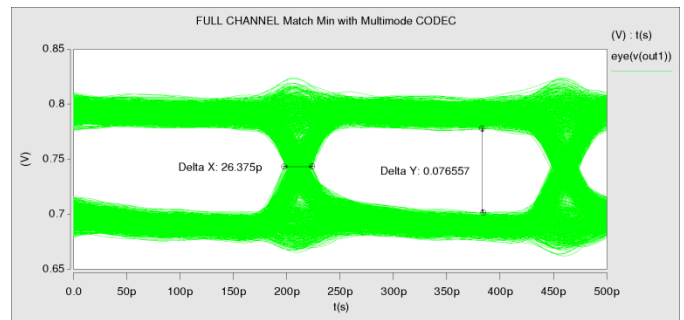


Figure 12. Full matched channel with multimode signaling.

To further optimize this channel, we tried to increase the spacing while keeping the characteristic impedance constant at 50Ω . By doing a sweep on the spacing, it is found that as the spacing increases, the eye height gets larger but the RMS jitter stays more or less the same. This trend holds until the spacing reaches $25 \mu\text{m}$, beyond which the eye height no longer improves significantly. For $25 \mu\text{m}$ spacing, the width is $36 \mu\text{m}$ to keep the characteristic impedance at 50Ω . With this setting, the eye diagram for the multimode signaling scheme is shown in Fig. 13. The eye height is 92 mV , increased by 48% compared with the initial minimum spacing setting that gives 62 mV . The RMS jitter is 26.7 ps , about the same as for the impedance match case with minimum spacing, which gives us a 63% reduction compared with the 73 ps with single-ended signaling.

To evaluate the overall performance of the optimized channel with multimode signaling, we compare it with the crosstalk free case, where only one line has active signals as shown in Fig. 14. The RMS jitter is 17% larger and the eye height is 13% lower compared with the absolutely crosstalk free scenario.

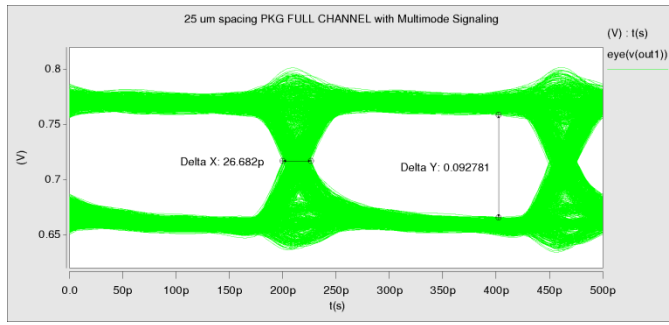


Figure 13. Full channel with optimum package for multimode signaling.

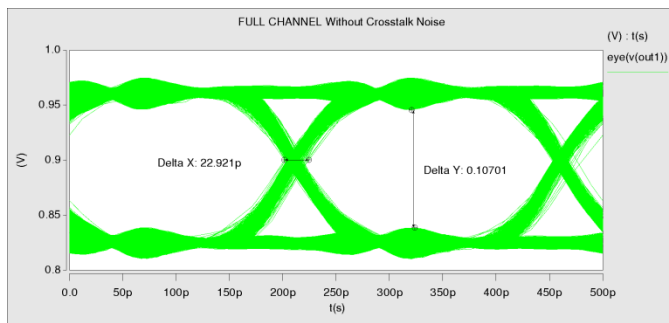


Figure 14. Eye diagram for crosstalk free full channel.

Improvements upon Benchmark Problem

In this section, to evaluate the potential of this work, we compare the optimized channel with a practical benchmark channel presented in [5]. The benchmark channel has symmetrical architecture comprised of two central processing unit (CPU) dies flip-chip assembled on two package substrates that reside on the opposite ends of the channel as depicted in Fig. 15.

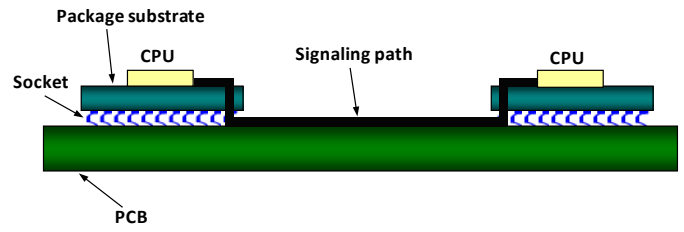


Figure 15. Channel components in the benchmark problem and the corresponding signal path.

First, let us compare the pitch of the benchmark channel with our optimized channel. For the PCB board main routing, the benchmark channel has a pitch of $800 \mu\text{m}$, while the optimized channel in this work has a pitch of $200 \mu\text{m}$ (width/spacing $100/100 \mu\text{m}$), which gives 300% density increase. For the signal routing on package, the pitch for the benchmark channel is $120 \mu\text{m}$, and the optimized channel has a pitch of $61 \mu\text{m}$ (width/spacing of $36/25 \mu\text{m}$), which gives us a 97% density increase.

The RMS jitter of this benchmark channel with multimode signaling is 39 ps which is 44% higher compared with the optimized channel that has 27 ps RMS jitter. Thus, even though the benchmark channel has additional discontinuities, the channel optimization demonstrated in the present paper has significant potential for increasing bandwidth density based on multimode signaling.

Conclusions

In this paper, a new circuit/channel co-design method for multimode signaling is proposed. With multimode signaling, the optimized channel shows over 60% jitter reduction compared with single-ended signaling. The optimized channel has 300% higher PCB routing density and 97% higher package routing density compared with a practical benchmark channel and still has 31% RMS jitter reduction as a result of multimode signaling. This optimized channel shows that this optimization process could greatly improve signal integrity and interconnect density with multimode signaling. Though no discontinuities such as socket, via, PTH etc. are discussed in this paper, the optimum design in the presence of these discontinuities can be explored with a similar optimization process.

Acknowledgements

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