**IRDS Emerging Research Devices and Architectures NanoCrossbar Workshop**

Date/time: 9-5, Friday July 15, 2016 at Rambus in Sunnyvale, CA

Moffet Towers, 1050 Enterprise Way #700, Sunnyvale CA 94089

Organizer: Paul D. Franzon, [paulf@ncsu.edu](mailto:paulf@ncsu.edu), 919 656 4411 (M)

Agenda:

Each presentation will consist of approximately 20 minutes of presentation and 20 minutes of discussion. Its OK if you go over 20 minutes. (Schedule subject to change).

0900– 0930 : Introduction: Paul Franzon, NC State University

0930 – 1020 : Matt Marinella, Sandia

1020 – 1040 : Break

1040 : 1120 : Geoff Burr IBM

1120 – 1200 : David Mountain, DOD (via Webex or phone) (cancelled)

1200 – 1300 : Lunch

1. – 1340 : Dmitri Strukov, UCSB
2. – 1420 : Kevin Cao, ASU

1420– 1440 : Break

1440 - 1520: Miao Hu, HPE

1520 – 1600 : Wei Lu, UMich

1600 – 1640 Gert Cauwenberghs, UCSD (via webex)

1640 – 1700 : Paul Franzon, Wrapup

Background

In the 2015 chapter, we identified that nanocrossbar arrays were coming close to being a deployable computing technology for neuromorphic, analog computing, and of memories. We wish to expand upon this section in the 2017 chapter. To that purpose, we are holding a work shop whose goes are as follows:

1. Identify and quantify the state of the art in devices, design, modeling, fabrication, and employment of Nano-enabled Crossbars for computing.
2. Identify the research barriers impeding the use of NanoCrossbars for computing.

Examples of questions that it would be helpful for you to consider addressing in your talk include the following.

General, including memories

* What is the status of achieving linear repeatable response, low power, sufficiently long retention, fast writes, sufficiently distinguishable resistances in different states, and long write endurance in one nanoscale device?
* Is the access device issue solved? What are the remaining issues?

Neuromorphic computing

* What are the requirements on device linearity, scalability and dynamic range?
  + What is achieved today?
  + What are the tradeoffs exposed in achieving this?
* What style of non-traditional computing is best suited to nanodevice arrays? E.g. spiking neuron, deep network, full logic map, etc.
  + Why?
  + What are the specific gaps in device properties that are preventing us from achieving this paradigm?

Analog computing

* What are the requirements on device linearity, scalability and dynamic range?
  + What is achieved today?
  + What are the tradeoffs exposed in achieving this?
* What is the required device yield? What mechanisms are available for implementing working arrays in the presence of <100% yield?
* What levels of noise during readout can be tolerated?
* To what degree could closed-loop control (e.g., iterative resistance-tuning for higher accuracy) be available during device write?