Chip-Package CoDesign
- Challenges and Directions

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Funding:
Outline

- High Density Packaging Trends
  - High density
  - 3-D
  - Embedded Passives
- Chip-Package Codesign Trends
- CAD Tools for Codesign
- Codesign CAD at NCSU
Package Technology Trends

▷ The trend to miniaturization
  - Wireless systems - COB, DCA
  - High pin-count systems
  - High speed interfaces (400 MHz)

▷ Packaging adding value to the system
  - High density, low-cost packaging
  - Three-D packaging
  - Embedded passives
  - Integration of sensors (MEMS)
High Density Packaging Trends

▶ Current technology:
  - 250 µm solder bump pitch
  - 50 µm wire pitch
  - 50 µm via pitch

▶ SHOCC Program
  - 50 µm solder bump pitch
  - 30 µm wire pitch

▶ Georgia Tech
  - Large panel processing
3-D MCM Design

New Ideas
• Low cost edge mounting technology
  • Invented at MCNC
  • Based on solder bumps
• Applications:
  • Self-aligning 3-D “null-seeking radar”
  • High density DRAM ‘SIMM’ module
  • MEMS, Analog integration

Impact
• Cost Reduction in low-weight high-density memories
• Self-aligning 3-D structures
  • Low cost
Integration of Sensors

**Examples:**
- RF Componentry
- Sensor/IC MCM
  - Accelerometers
  - LiDAR

**Challenges**
- Packaging cost > MEMS cost
- Test cost > MEMS cost
- Codesign of MEMS and analog/digital signal processing
Outline

High Density Packaging Trends

Chip-Package Codesign Trends

CAD Tools for Codesign

Codesign CAD at NCSU

• NCSU
• Alpine
• Lucent
Co-Design for Flip Chip & thin-film

New Ideas

• Use low-R HDI copper for:
  • on-chip power/ground distn
  • 1-level clock distribution
  • RAM interfacing
• Build high BW memory systems
  • 512-bit buses
  • 800 Mbps I/O signalling

Impact

• 5% - 30% IC size reduction
• 150 ps clock skew reduction
• 25% clock power reduction
• Improved noise management
• High bandwidth memory for DSP

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Optimizing the Interconnect Mix

- Low-cost, high-density interconnect technologies

**IC:**
- 6-7 copper layers:
  - 150 to 2,000 nm thick
  - sub-micron pitch

**Solder Bump:** 50 to 250 micron pitch

**HDI:**
- 4+ copper layers
  - 4,000 to 16,000 nm thick
  - 30 to 50 micron pitch

**Integrated Decoupling:**
- 700 - 10,000 pF/sq.cm.
Triple-DES Module

Data Encryption Standard Module - Encrypt, Decrypt, and Cracking
IC Implementation

- CMOS three metal, 0.6µm technology
- Test structures: full scan, PRNG, SAR
- 123,104 transistors
- 210 pads used
  - inputs: 18 clock, 15 control, 64 data
  - outputs: 67
  - power: 23, ground: 23
- 5.78mm X 3.67mm (21.2mm²)
- Global P/G/C distribution is provided by MCM
Implementation: The Chip
Area Array P/G/Clock Distribution

- eliminates large global rails
Power Distribution Architecture

Integrated Decoupling Capacitors
- MCM = 700 - 10,000 pF/sq.cm.
- IC = 2.5 - 5.0 pF/sq.mm.
  (at 5% fill: 12.5 - 25 pF/sq.cm)

Would not work for MCM-C/L:
- via inductance too high
  (0.05 nH vs. 0.5 nH)
Power Distribution - IR drop

High density solder bumping releases on-chip wiring resources.

Requirements to keep IR drop to 15 mV.
Global Clock Distribution

- Distribute Global Clock on low-R MCM layers
  - Reduced clock skew (shallower clock tree)
  - Reduced clock power (smaller crowbar current)
  - Transmission line distribution schemes
Global Clock Distribution

- i.e. For conventional clock trees:

PLL/Driver

- On-chip Clock wiring
- On-MCM Clock wiring
Laboratory Test Equipment Setup

- Logic Analyzer
- TLA 216 Logic Scope
- PC and HFS 9009 Stimulus Generator
- DPO Oscilloscope
- DUT
Probing the MCM

- High-impedance active probe for measuring Vdd noise and clock skew
Measured IC Performance (Speed)

Results:

- 110 MHz
- 2.5 GBps encrypt/decrypt
DES MCM Power Plane Noise

Vdd plane/clock buffer voltage (3 chips running, decoupling added)
DES MCM  Power Plane Noise

![Graph of Vdd plane voltage over time with different numbers of chips running.]
DES MCM Power Plane Noise
Clock Distribution - DES MCM

Clock input at H-tree leaf, f=50MHz
Clock Distribution - DES MCM

Clock input at H-tree leaf, f=50MHz

- leaf B8, chip 2
- leaf A1, chip 1
GCLK Distribution on MCM

25% GCLK Power Reduction when GCLK distributed on MCM

Global Clock (GCLK) Distribution - Goals

- GCLK Performance Goals:
  - Low Skew (≤ 50ps)
  - Uniform Rise/Fall Times
  - 48% to 52% Duty Cycle

- Other Clock Related Goals:
  - Reduced Power Supply Collapse
  - Uniform Die Temperature
  - Easily Tunable

Final GCLK Driver

GCLK Distribution Network
SSN Measurement IC

Addresses on-chip noise issues in flip-chip environment

- Core noise contribution significant
- Greater on-chip exposure to SSN
- Intend to produce suitable macromodels
Alpine Systems

Achieving greatly decreased footprint with careful codesign across multiple levels of interconnect

2,000 I/O pins in a 256-pin BGA
Embedded Passives

Frye, Lucent, Bell Labs
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• Current Status
• Future Needs
Packaging CAD Status

IC and package tools very separated:

IC Physical Design

Package Physical Design

IC I/O Locations

Package Modeling/Simulation

On IC Modeling/Simulation

Franzon
Packaging CAD Status

Current points of integration concentrate on single net SI and routability, mainly at the board level

- e.g. Xinetix EDA Navigator or Cadence SpectraQuest
Future Design Issues

preneur noise issues becoming critical
   - Requires co-modeling of chip and package

Routing Resources becoming very tight
   - Flip-chip breakout can be difficult
   - On-chip interconnect dominating on-chip delays
   - Miniaturization in RF systems leads to very constrained board designs

Must seek codesign opportunities
   - Digital - optimal interconnect allocation
   - Analog - embedded passives
   - Must include process variations of chip and package
Breakout Issues

To breakout a large number of pads with a river route requires intensive routing resources:

Top View

Cross-Section

Solder Bumps
Signal Layers
Ref. plane

Need more signal layers to break out more pins
Possible Future Flow

IC Physical Design
- Floorplanner
- Net planner

Package Physical Tools
- Preliminary Layout
- Net planner

Pad locations
Circuit (driver) Models
- process variations
On-chip delay range
Noise susceptibility

Back-Annotation

Routability
- Breakout
Package delay

Automatic I/O placement tool

Back-Annotation
...Possible Future Flow

IC Extraction and Analysis Tools
- SSN Macromodels
- On-chip Noise Margin Requirements

Signal Integrity and Performance Analysis
- On-chip SI
- Off-chip SI
- Performance verification (across process and temp)

Packaging Extraction Tools
- Package parasitics
- Inter-chip Noise Margin Requirements

Back-Annotation
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Concentrating on on-chip block and I/O placement
Performance Driven IC-placement

Goals:
- Place on-IC blocks and I/O to
  - minimize longest delay
  - ensure routability

Approach
- Simulated annealing placement
- Weighted Trunk Tree length estimator
- Delay mean and standard deviation used in objective function
- Routing Resource Metric used in objective function
Weighted Trunk Tree Length

- Results lengths within 1% of Cadence silicon ensemble actual lengths. (Other methods typically 5% accurate.)

\[
x_{wty} = \frac{1}{N} \sum_{i=1}^{N} x_i
\]

\[
y_{wty} = \frac{1}{N} \sum_{i=1}^{N} y_i
\]

\[
L_{wtx} = \text{diam}(x) + \sum_{i=1}^{N} |y_i - y_{wtx}|
\]

\[
L_{wty} = \text{diam}(y) + \sum_{i=1}^{N} |x_i - x_{wtx}|
\]

\[
diam(x) = \max\{x_i\} - \min\{x_i\}
\]

\[
diam(y) = \max\{y_i\} - \min\{y_i\}
\]

\[
L_{WTT} = \frac{1}{2}(L_{wtx} + L_{wty})
\]
Routability Estimation

Routing Resource Metric

\[ RRM = \frac{A_T - K_M A_M}{\lambda_W L_T} \]

- \( A_T \): Total routing area
- \( A_M \): Area occupied by modules
- \( K_M \): Utilization factor of modules for routing
- \( L_T \): Total Estimated interconnect length (WTT)
- \( \lambda_W \): Effective wire pitch
Results

Placed and routed ten experiments (routing using Cadence Silicon Ensemble)

- Designs 1.3x faster on average than with conventional methods
- Faster convergence on correct design - One iteration in each case
Conclusions

- The relationship between electronic packaging design and IC design is becoming strong:
  - Package adding value to IC
  - Package noise affecting IC design
  - High pin count systems

- New design approaches and tools are needed
  - Codesign across disciplines
  - Integrated tool flows to solve important problems
Performance-drive IC placement

New Ideas:
- Estimators
  - Weighted Trunk Tree (WTT)
  - Pre-characterized Delay Models
  - Routing Resource Metric (RRM)
- Dynamic Path-Delay Minimization

Impact:
- Sample Designs are 1.3x faster
- No timing violations after first iteration between placement and detailed routing

Yusuf Tekmen, Real Pommerleau, Paul Franzon, Griff Bilbro
High Density Packaging Trends

▷ Short Term
  ◆ Increased penetration of Direct Chip Attach (DCA) (solder balls) and Chip-On-Board (COB)
    ◇ Increased scope for package-induced SSN noise impacting on-chip design and functionality
    ◇ Layout difficulties in high pin count systems
  ◆ High speed interfaces require careful codesign of chip and package
    ◇ 400 MHz buses becoming common

▷ Long Term
  ◆ Package technology *adding value* to the system
    ◇ High density, low-cost packaging
    ◇ Embedded passives
Clock Distribution

- On-MCM H-tree removes level of clock tree, eliminating up to 150ps of process-induced skew
High Density Packaging Trends

- Reduced Chip Test Cost for High I/O Chips

2,000 I/O
Membrane tester
Examples of Emerging Design Styles

- Integrated IC-package functionality
  - NCSU work
  - Alpine Systems
  - Lucent RF Module (above)

Figure 5: RF module design using MCM-D substrate technology and flip-chip assembly.
Future Design Opportunities

- **Mixed Signal**
  - First-pass design success very difficult, and even more difficult with embedded passives
  - Issues:
    - System Modeling
    - Co-simulation
    - Independent Process Variations

- **Mixed Technology**
  - MEMS
  - Sensors in general
    - System Modeling Problem
Solution Paths

- Take Lead from IC World:

- Flows - tightly integrated tool sets to solve particular problems

- e.g. Possible I/O Planner Flow for flip-chip, thin-film packages

  - Problems being addressed:
    - Signal integrity due to on-chip and on-package noise
    - I/O placement to satisfy performance and routability
Discussion

Why will a flow like this be important?

- On-chip noise dominated by package issues
- Ensure first time success in:
  - High pin count designs
  - Mixed-signal Systems

A flow like this is difficult

- Tightly integrated heterogeneous tool set
- Different vendors
- Point tools not designed with flows in mind
High bandwidth MEMS-switches

New Ideas

• Low Impedance MEMS programmable capacitor ‘switches’
• Pulse signaling through programmable capacitor array
• Each MEMS switch individually controllable via row and column addressing only

Impact

• 1 Gbps crossbar
  • 32x32 to 196x196
• Suitable as RF switches also:
  • Phased array for low cost radars and directional wireless communications
MEMS-based laser radar

New Ideas
- Programmable hologram based on MEMS array
- 6 degrees of steering
- Organized as >400 8x8 subarrays
- Each subarray requires 8 address lines only

Impact
- Makes laser radar feasible
  - ‘fine’ steering capability
  - adaptive optics
- Potential for
  - 3D machine vision
  - optical interconnect

Jeremy Palmer, David Winick