Plenary Talk

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On why dielets are the new craze for heterogeneous Integration

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<Abstract>
Chiplets (or more accurately dielets) are the new thing in heterogeneous systems integration. In this talk, we will review why this makes sense and what the criteria for dielet selection are. Dielet selection depends on functionality and reuse potential but and are constrained by yield, handling and testing. This limits the die size to between 1 and 100 mm2. The technologies that will be used to implent this concept are diverse and application dependent. They willl require new substrate and assembly technologies. The dielet approach has significant challenges in both the infrastructure as well as the ecosystem. These include a secure supply chain and diversity of dielets. We'll discuss those as well. We will introduce two heterogeneous integration platforms the SiIF and Flextrate to demonstrate these ideas. The dielet concept is gaining momentum and offers a good way to leverage the solid existing semiconductor infrastructure and make advanced packaging a much more value-add component of the technology.

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Subramanian S. Iyer (Subu) is Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at the University of California at Los Angeles. He is Director of the Center for Heterogeneous Integration and Performance Scaling (CHIPS). Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world's first SiGe base HBT, Salicide, electrical fuses, embedded DRAM and 45nm technology node used to make the first generation of truly low power portable devices as well as the first commercial interposer and 3D integrated products. He also was among the first to commercialize bonded SOI for CMOS applications through a start-up called SiBond LLC. More recently, he has been exploring new packaging paradigms and architectures that they may enable including in-memory analog compute. He has published over 300 papers and holds over 70 patents. He was a Master Inventor at IBM. He has received several outstanding technical achievements and corporate awards at IBM. He is an IEEE Fellow, an APS Fellow and a Distinguished Lecturer of the IEEE EDS and EPS as well as the treasurer of EDS and a member of the Board of Governors of IEEE EPS. He is also a Fellow of the National Academy of Inventors. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012.
List of publications/patents:
https://scholar.google.com/citations?user=xXV4oIMAAAAJ&hl=en