IEEE 2019 INTERNATIONAL 3D SYSTEMS INTEGRATION CONFERENCE
October 8-10, 2019 Sendai, Japan
October 8 at Hotel Metropolitan Sendai
October 9-10 at Miyagino Ward Cultural Center, Sendai

Invited Talk

15:00-15:30, 09-Oct-19 Paper ID-4085

An Introduction to Marching Memory (MM)

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<Abstract>
Today's computer systems rather have a "big issue," which is what is called the memory bottleneck, especially as their scale has been growing with nanotechnology year by year toward EXA-scale supercomputing for scientific calculations and deep learning in neural-networking. In modern computers, there exists mostly "serial data transfer" between memories and not random data transfer. Between HDD/ Flash and DDRx-DRAM there is a page that is a group of bytes transferred as a single unit. Between DDRx-DRAM and caches, there is a cache line (line) that is a group of bytes transferred as a single unit. Even between a cache and a register file, the data transfer might be serial with cache lines. So, to drive existing computers faster with we introduce a new super memory "Marching Memory (MM)." The speed of MM is much faster than DRAM's and even SRAM's at lower power even though depending on applications. The feature of this is structurally speedup of accessing with high bandwidth and without delay. In case of MM, there is no addressing but it locates, without access protocols, an aimed memory location by data marching "column by column" within MM at a high speed. Thinking of all sorts of memories in general purpose computers, caches L1, L2 and L3 are the most suitable ones to be replaced with MM because these caches are constructed of SRAM that is not faster than MM and the power consumption is larger than MM's. Especially in supercomputers the vector register could be replaced with MM, and a computer for deep learning expects high bandwidth with MM. As a result, MM could contribute to speedup of many computers with lower power.

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Tadao Nakamura received his PhD from Tohoku University in 1972. He was a Full Professor at Tohoku University from 1988-to 2007, and sent out internationally his many PhD graduates to universities and industries. He is a Professor Emeritus of Tohoku University, and also has been a Professor (as a visiting status) of Keio University since 2007. Especially in 1994 he was given the status of a Full Professor (Principal of Stanford Computer Architecture as a visiting status) in the Electrical Engineering Department at Stanford University. And even today he still stays at Stanford University at any time because he with Professor Michael J. Flynn has been creating the new concept of much higher speed memory with lower power consumption, named Marching Memory (MM), to avoid the memory bottleneck in computer systems. In 2007 he was also induced as a Professorial Fellow at Imperial College London. Meanwhile, as for lectures, he worked at Cambridge University in England, The University of Michigan, and The University of Tokyo in suitable positions such as a guest professor. His research interests are toward computer systems. In 2004 he received the IEEE Computer Society's Taylor L. Booth Award. He has been Steering Committee Chair, after the Organizing Committee Chair and Advisory Committee Chair of COOL Chips conference series fully sponsored by the IEEE Computer Society. He is Life Fellow of the IEEE.