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*October 8 at Hotel Metropolitan Sendai*  
*October 9-10 at Miyagino Ward Cultural Center, Sendai*

## Invited Talk

**16:55-17:25, 09-Oct-19 Paper ID-4077**

### **Monolithic 3D as an alternative to advanced CMOS scaling: technology, design and architecture perspectives**

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#### **<Abstract>**

Monolithic 3D technology (M3D) is a promising alternative to tackle the loss of Moore's Law scaling beyond 22 nm node. By stacking different circuit layers thanks to nano-scale 3D Monolithic Inter Tier Via (MITV), it will be possible to offer a level of circuit integration never reached before, allowing advanced node scaling again as well as mixing heterogeneous technologies. M3D integrates sequentially different layers of transistors, with an ultra-fine pitch, in the 100 nm range, which is 200x smaller than state-of-the-art Through Silicon Vias (TSV) or 50x smaller than Copper to Copper Hybrid bonding (Cu-Cu HB). This high density 3D integration will pave the way towards new architectures, such as neuro- and bio-inspired applications, ultra-high density memory-computing cube and smarter mixed signal devices within tight low power constraints. This talk presents an overview of M3D technology and potential applications, and in more detail its associated design challenges, respectively on physical implementation aspects and on thermal dissipation.

#### **<CV>**

Dr Pascal Vivet is Scientific Director of the Architecture, IC Design and Embedded Software Division in CEA-LETTI, Grenoble, France. He received his PhD from Grenoble Polytechnical Institute in 2001, designing an asynchronous microprocessor. After 4 years within STMicroelectronics, he joined CEA-Leti in 2003 in the digital design lab. His research interests covers wide aspects of circuit and system level design, ranging from system integration, multi-core architecture, Network-on-Chip, energy efficient design, related CAD design aspects, and in strong links with advanced technologies such as 3D integration, Non-Volatile-Memories, photonics. He was project leader on 3D circuit design and integration since 2011. He participates to various TPC such as ASYNC, DATE, 3DIC conferences. He served as a member of the organizing committee of the 3D workshops series at DATE from 2013 to 2015, and to the D43D workshops since 2011. He has authored and co-authored more than 80 papers and holds several patents in the field of digital design. He co-authored a book chapter on "3D Integration in VLSI Circuits: Implementation Technologies and Applications.