Aug. 31 (Mon)

Sendai International Center 7:30 –

Registration

Room: Tachibana Conference Hall 8:30 – 8:50

Opening Ceremony

Room: Tachibana Conference Hall 8:50 – 9:35

Keynote (I)

3D-IC Technologies and 3D FPGA

Xin Wu
Silicon Technology, Xilinx INC, San Jose, California, USA

Break (9:35 – 9:50)

Room: Tachibana Conference Hall 9:50 – 11:15

Technical Session (I) <3D Integration Technologies>

I-1 Invited Talk: Some Challenges in Scaling 3D ICs to a Broader Application Set

Subramanian Iyer
University of California at Los Angeles, USA

I-2 Reconfigured Multichip-on-wafer (mCoW) Cu/oxide Hybrid Bonding Technology for Ultra-high Density 3D Integration Using Recessed Oxide, Thin Glue Adhesive, and Thin Metal Capping Layers

Kangwook Lee[1, 2], Chisato Nagai[1], Ai Nakamura[1], H. Aizawa[1], H. Hashiguchi[3], Jicheol Bea[1, 2], Takafumi Fukushima[1, 2], Tetsu Tanaka[3], Mitsumasa Koyanagi[1, 2]
[1]NICHe, Tohoku University, Japan, [2]GINTI, Tohoku University, Japan, [3]Dept. of Biomedical Engineering, Tohoku University, Japan

I-3 Intermediate BEOL Process Influence on Power and Performance for 3DVLSI

Hossam Sarhan[1], Sebastien Thuries[1], Olivier Billoint[1], Fabien Deprat[1], Alexandre Ayres De Sousa[1, 2], Perrine Batude[1], Claire Fenouillet-Beranger[1], Fabien Clermidy[1]
[1]Univ. Grenoble Alpes, F-38000 Grenoble, France, CEA, LETI, MINATEC Campus, F-38054 Grenoble, France, [2]STMicroelectronics, F-38926 Crolles, France

Aug. 31 (Mon)

I-4 **Silicon Based Dry-Films Evaluation for 2.5D and 3D Wafer-level System Integration Improvement**

Amandine Jouve[1], Yann Sinquin[1], Arnaud Garnier[1], Marion Daval[1], Pascal Chausse[1], Maxime Argoud[1], Nacima Allouti[1], Laurence Baud[1], Jerome Dechamp[1], Remi Franiatte[1], Severine Cheramy[1], H.Kato[2], K. Kondo[2]
[1]CEA, LETI, Minatec Campus, FRANCE, [2]Shin-Etsu Chemical Corp., Gunma 379-0224, Japan

Room: Tachibana Conference Hall	11:15 – 12:20

Technical Session (II) <3D DRAM (1)>

II-1 **Invited Talk: Progress in 3D Integrated Circuits**

Robert Patti
Tezzaron Semiconductor Corp., USA

II-2 **Electrical Performance of High Bandwidth Memory (HBM) Interposer Channel in Terabyte/s Bandwidth Graphics Module**

Hyunsuk Lee, Kyungjun Cho, Heegon Kim, Sumin Choi, Jaemin Lim, Joungho Kim
Korea Advanced Institute of Science and Technology, Korea

II-3 **New Signal Skew Cancellation Method for 2G bps Transmission in Glass and Organic Interposers to Achieve 2.5D Package Employing Next Generation High Bandwidth Memory (HBM)**

Syuuichi Kariyazaki[1], Kenichi Kuboyama[2], Ryuichi Oikawa[1], Takuo Funaya[1]
[1]System Assembly Solution Department, Renesas Electronics Corporation, Japan, [2]ICT Control System Development Department, Renesas System Design Corporation, Japan

Lunch (12:20 – 13:40)

Room: Tachibana Conference Hall	13:40 – 14:20

Technical Session (III) <3D DRAM (2)>

III-1 **Novel Local Stress Evaluation Method in 3D IC Using DRAM Cell Array with Planar MOS Capacitors**

Seiya Tanikawa[1], Hisashi Kino[2], Takafumi Fukushima[1], Mitsumasa Koyanagi[3], Tetsu Tanaka[1, 4]
[1]Department of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University, Japan, [2]Frontier Research Institute for Interdisciplinary Sciences, Tohoku University, Japan, [3]New Industry Creation Hatchery Center, Tohoku University, Japan, [4]Department of Biomedical Engineering, Graduate School of Biomedical Engineering, Tohoku University, Japan

III-2 **Characterization of Stress Distribution in Ultra-thinned DRAM Wafer**

Tomoji Nakamura[1, 2], Yoriko Mizushima[1, 2], Young Suk Kim[2], Ryuichi Sugie[3], Takayuki Ohba[2]
[1]Fujitsu laboratories Ltd., Japan, [2]Tokyo Institute of Technology, Japan, [3]Toray Research Center, Inc., Japan

Aug. 31 (Mon)

Room: Tachibana Conference Hall **14:20 – 15:00**

Technical Session (IV) <Cu Metallization>

IV-1 **No Pumping at 450°C with Electrodeposited Copper TSV**

Kazuo Kondo[1], Shingo Mukahara[1], Jin Onuki[2], Masayuki Yokoi[1]
[1]Dept. of Chemical Engineering, Osaka Prefecture University, Japan, [2]Department of Materials Engineering, Ibaragi University, Japan

IV-2 **Thermal Stability of Electroplated Copper Thin-film Interconnections**

Pornvitoo Rittinon[1], Ken Suzuki[2], Hideo Miura[2]
[1]Department of Nanomechanics, Tohoku University, Japan, [2]Fracture and Reliability Research Institute, Tohoku University, Japan

Break (15:00 – 15:15)

Room: Tachibana Conference Hall **15:15 – 17:45**

Focus Session and Panel Discussion <3D Research Activities>

FS-1 **3D System Integration Program Research at IMEC**

Eric Beyne
IMEC, Belgium

FS-2 **Advanced 2.5D/3D Hetero-Integration Technologies at GINTI, Tohoku University**

Kangwook Lee[1, 2], Jicheol Bea[1, 2], Takafumi Fukushima[1, 3], Tetsu Tanaka[1, 3], Mitsumasa Koyanagi[1, 2]
[1]GINTI, Tohoku University, Japan, [2]NICHe, Tohoku University, Japan, [3]Dept. of Biomedical Engineering, Tohoku University, Japan

FS-3 **3D Research Activities in ITRI**

Wei-Chung Lo
ITRI, Taiwan

FS-4 **Current and Future 3D Activities at Fraunhofer**

Andy Heinig[1], Muhammad Waqas Chaudhary[1], Peter Schneider[1], Peter Ramm[2], Josef Weber[2]
[1]Fraunhofer Institute for Integrated Circuits, Design Automation Division, Dresden, Germany, [2]Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT, Munich, Germany

FS-5 **IME's Capabilities and Programs in 2.5D/3DIC**

Vempati Srinivasa Rao
Institute of Microelectronics, Singapore

FS-6 **3D Advanced Integration Technology for Heterogeneous Systems**

Pascal Vivet, Christian Bernard, Fabien Clermidy, Denis Dutoit, Eric Guthmuller, Ivan-Miro Panadès, G. Pillonnet, Yvain Thonnart, Arnaud Garnier, Didier Lattard, Amandine Jouve, Franck Bana, Thierry Mourier, Séverine Chéramy
CEA LETI, France

Aug. 31 (Mon)

FS-7 **Path to 3D Heterogeneous Integration**

Daniel S. Green[1], Carl L. Dohrman[2], Jeffrey Demmin[2], Tsu-Hsi Chang[3]
[1]DARPA, USA, [2]Booz Allen Hamilton, Inc., Arlington, VA 22203, USA, [3]HetInTec Corp.; Rockville, MD 20850, USA

Westin Hotel Sendai	**18:30 – 20:30**

Banquet

Sep. 1 (Tue)

Sendai International Center **8:00 –**

Registration

Room: Tachibana Conference Hall **8:30 – 9:15**

Keynote (II)

The Issues of Automated Driving Vehicle and the Expectations for 3D Integration Technology

Tadashi Kamada
DENSO CORPORATION Advanced Research Division, Social Science Research Department, Japan

Room: Tachibana Conference Hall **9:15 – 10:40**

Technical Session (V) <New TSV Materials>

V-1 **Invited Talk: 3D Integration: Applications and Market Trends**

Rozalia Beica
Yole Développement, France

V-2 **Vacuum-assisted-spin-coating of Polyimide Liner for High-aspect-ratio TSVs Applications**

Yangyang Yan[1, 2], Yingtao Ding[1], Qianwen Chen[1], Kangwook Lee[2], Takafumi Fukushima[2], Mitsumasa Koyanagi[2]
[1]Beijing Institute of Technology, China, [2]Tohoku University, Japan

V-3 **Nano-function Materials for TSV Technologies**

Hiroaki Ikeda[1, 2], Shigenobu Sekine[1], Ryuji Kimura[1], Koichi Shimokawa[1], Keiji Okada[1], Hiroaki Shindo[1], Tatsuya Ooi[1], Rei Tamaki[1], Makoto Nagata[2]
[1]Napra Co. Ltd., Japan, [2]Graduate School of System Informatics, Kobe University, Japan

V-4 **High-speed Via Hole Filling Using Electrophoresis of Ag Nanoparticles**

Ryo Takigawa[1], Kohei Nitta[1], Akihiro Ikeda[1], Mitsuaki Kumazawa[2], Toshiharu Hirai[2], Michio Komatsu[2], Tanemasa Asano[1]
[1]Kyushu University, Japan, [2]JGC Catalysts Chemicals LTD, Japan

Break (10:40 – 10:55)

Sep. 1 (Tue)

Room: Tachibana Conference Hall 10:55 – 12:20

Technical Session (VI) <3D System Related Technologies>

VI-1 Invited Talk: Computing in 3D

Paul D. Franzon, Eric Rotenberg, W. Rhett Davis, James Tuck, W. Rhett Davis, Huiyang Zhou, Joshua Schabel, Zhenquian Zhang, J. Brandon Dwiel, Elliott Forbes, JoonmooHuh, Marcus Tshibangu, Steve Lipa
Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, USA

VI-2 Comprehensive Comparison of 3D-TSV Integrated Solid-State Drives (SSDs) with Storage Class Memory and NAND Flash Memory

Shogo Hachiya, Takahiro Onagi, Sheyang Ning, Ken Takeuchi
Chuo University, Japan

VI-3 Power Saving and Noise Reduction of 28nm CMOS RF System Integration Using Integrated Fan-out Wafer Level Packaging (InFO-WLP) Technology

Chuei-Tang Wang, Jeng-Shien Hsieh, Victor C. Y. Chang, En-Hsiang Yeh, Feng-Wei Kuo, Hsu-Hsien Chen, Chih-Hua Chen, Ron Chen, Ying-Ta Lu, Chewn-Pu Jou, Hao-Yi Tsai, C. S. Liu, Doug C. H. Yu
R&D, TSMC, Ltd., Taiwan

VI-4 3D ICs: An Opportunity for Fully-integrated, Dense and Efficient Power Supplies

Gaël Pillonnet[1], Nicolas Jeanniot[1, 2], Pascal Vivet[1]
[1]Univ. Grenoble Alpes, F-38000 Grenoble, France CEA, LETI, MINATEC Campus, F-38054 Grenoble, France,
[2]Univ. of Lyon, CPE Department, F-69616, Villeurbanne, France

Lunch (12:20 – 13:40)

Room: Tachibana Conference Hall 13:40 – 15:05

Technical Session (VII) <Wafer Bonding/Chip Stacking>

VII-1 Invited Talk: New Precision Wafer Bonding Technologies for 3DIC

Isao Sugaya[1], Hajime Mitsuishi[1], Hidehiro Maeda[1], Kazuya Okamoto[1, 2]
[1]Nikon, Japan, [2]Osaka University, Japan

VII-2 Permanent Wafer Bonding in the Low Temperature by Using Various Plasma Enhanced Chemical Vapour Deposition Dielectrics

Soon-Wook Kim[1], Lan Peng[1], Chung Sun Lee[2], Andy Miller[1], Gerald Beyer[1], Eric Beyne[1]
[1]IMEC, Belgium, [2]Samsung Electronics, Korea

VII-3 High Productivity Thermal Compression Bonding for 3D-IC

Noboru Asahi, Yoshinori Miyamoto, Masatsugu Nimura, Yoshihito Mizutani, Yoshiyuki Arai
Solution Center Research & Development Div. Toray Engineering Co., Ltd, Japan

VII-4 Transfer and Non-transfer Stacking Technologies Based on Chip-to-wafer Self-assembly for High-throughput and High-precision Alignment and Microbump Bonding

Takafumi Fukushima[1, 2], Taku Suzuki[3], Hideto Hashiguchi[1], Chisato Nagai[2], Jichoel Bea[2], Hiroyuki Hashimoto[2], Mariappan Murugesan[2], Kangwook Lee[2], Tetsu Tanaka[1, 4], Kazushi Asami[3], Yasuhiro Kitamura[3], Mitsumasa Koyanagi[2]

[1]Department of Bioengineering and Robotics, Tohoku University, Japan, [2]Global INTegration Initiative (GINTI), New Industry Creation Hatchery Center, Tohoku University, Japan, [3]Research Laboratories, DENSO CORPORATION, Japan, [4]Department of Biomedical Engineering, Tohoku University, Japan

Room: Sakura Hall 1 15:05 – 16:35

Technical Session (VIII) [Poster Session]

VIII-1 Copper-filled Anodized Aluminum Oxide - A Potential Material for Chip to Chip Bonding -

Kosuke Yamashita, Shunji Kurooka, Koji Shirakawa, Yoshinori Hotta, Hirofumi Abe

Electronic Materials Research Laboratories, FUJIFILM Corporation, Japan

VIII-2 Development of High-quality Low-temperature (≤ 120°C) PECVD-SiN Films by Organosilane

Hiroshi Taka[1], Katsumasa Suzuki[1], Norihiro Tsujioka[2], Shoichi Murakami[2]

[1]TAIYO NIPPON SANSO Corporation, Japan, [2]SPP Technologies Co.,Ltd., Japan

VIII-3 Vertical Integration after Stacking (ViaS) Process for Low-cost and Low-stress 3D Silicon Integration

Kuniaki Sueoka, Akihiro Horibe, Toyohiro Aoki, Sayuri Kohara, Kazushige Toriyama, Hiroyuki Mori, Yasumitsu Orii

IBM Research - Tokyo, Japan

VIII-4 All-wet TSV Filling with Highly Adhesive Displacement Plated Cu Seed Layer

Kohei Ohta, Atsushi Hirate, Yuto Miyachi, Tomohiro Shimizu, Shoso Shingubara

Graduate school of science and engineering, Kansai University, Japan

VIII-5 Variation of Thermal Stress in TSV Structures Caused by Crystallinity of Electroplated Copper Interconnections

Jiatong Liu[1], Ryosuke Furuya, Ken Suzuki[2], Hideo Miura[2]

[1]Department of Nanomechanics, Tohoku University, Japan, [2]Fracture and Reliability Research Institute, Tohoku University, Japan

VIII-6 Twice-Etched Silicon Approach for Via-Last Through-Silicon-Via with a Parylene-HT Liner

Tung T. Bui, Naoya Watanabe, Masahiro Aoyagi, Katsuya Kikuchi

Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology, Japan

VIII-7 Air-Gap/SiO2 Liner TSVs with Improved Electrical Performance

Cui Huang, Dong Wu, Liyang Pan, Zheyao Wang

Institute of Microelectronics, Tsinghua University, China

Sep. 1 (Tue)

VIII-8 An Ultra-Fast Temporary Bonding and Release Process Based on Thin Photolysis Polymer in 3D Integration

Tsung Yen Tsai[1], Chien Hung Lin[2], Chia Lin Lee[2], Shan Chun Yang[2], Kuan Neng Chen[1]
[1]Department of Electronics Engineering, National Chiao Tung University, Taiwan, [2]Semiconductor Technology R&D Department, Kingyoup Optronics Co., Ltd., Taiwan

VIII-9 Copper Micro and Nano Particles Mixture for 3D Interconnections Application

Yuan Yuan Dai[1, 3], Mei Zhen Ng[2, 3], Anantha P[1, 3], Chee Lip Gan[2, 3], Chuan Seng Tan[1, 3]
[1]School of Electrical & Electronic Engineering, Nanyang Technological University, Singapore , [2]School of Materials Science and Engineering, Nanyang Technological University, Singapore , [3]NTU-Lockheed Martin Joint Lab, Nanyang Technological University, Singapore

VIII-10 Mitigating Thermo Mechanical Stress in High-density 3D-LSI Through Dielectric Liners in Cu-Through Silicon Via - μ-RS and μ-XRD Study

Murugesan Murugesan[1], Takafumi Fukushima[2], JiChel Bea[1], H. Hashimoto[1], KangWook Lee[1], Tetsu Tanaka[2], Mitsumasa Koyanagi[1]
[1]Global INTegration Institute (GINTI), NICHE, Tohoku Univ., 6-6-10, Aramaki, Aoba-ku, Sendai, 980-8579, Miyagi, Japan, [2]Department of Biomedical Engineering, Tohoku Univ., 6-6-12, Aramaki, Aoba-ku, Sendai, 980-8579, Miyagi, Japan

VIII-11 TSV Etching and VDP Process Integration for High Reliability

Takahide Murayama, Yasuhiro Morikawa
ULVAC Inc., Institute of Semiconductor and Electronics Technologies, Japan

VIII-12 Electrical Investigation of Cu Pumping in Through-Silicon Vias for BEOL Reliability in 3D Integration

Chuan-An Cheng[1], Ryuichi Sugie[2], Tomoyuki Uchida[2], Kuo-Hua Chen[3], Chi-Tsung Chiu[3], Kuan-Neng Chen[1]
[1]Department of Electronics Engineering, National Chiao Tung University, Taiwan, [2]Toray Research Center Inc., Japan, [3]Advanced Semiconductor Engineering Group, Taiwan

VIII-13 Long Term Efficacy of Ultrathin Ti Passivation Layer for Achieving Low Temperature, Low Pressure Cu-Cu Wafer-on-Wafer Bonding

Asisa Kumar Panigrahi, Satish Bonam, Tamal Ghosh, Siva Rama Krishna Vanjari, Shiv Govind Singh
Department of Electrical Engineering Indian Institute of Technology,Hyderabad, India

VIII-14 Fast Filling of Through-silicon Via (TSV) with Conductive Polymer/metal Composites

Jin Kawakita, Barbara Horvath, Toyohiro Chikyow
National Institute for Materials Science, Japan

VIII-15 Room-temperature Bonding Mechanism of Compliant Bump with Ultrasonic Assist

Keiichiro Iwanabe, Tanemasa Asano
Graduate School of Information Science and Electrical Engineering, Kyushu University, Japan

VIII-16 Influential Factors in Low-temperature Direct Bonding of Silicon Dioxide

Ryouya Shirahama, Sethavut Duangchan, Yusuke Koishikawa, Akiyoshi Baba
Center for Microelectronic Systems, Kyushu Institute of Technology, Japan

VIII-17 Warpage Analysis of Organic Substrates for 2.1D Packaging

Sayuri Kohara, Keishi Okamoto, Hirokazu Noma, Kazushige Toriyama, Hiroyuki Mori
IBM Research-Tokyo, Japan

Sep. 1 (Tue)

VIII-18 Guard-Ring Monitoring System for Inspecting Defects in TSV-Based Data Buses

Yuuki Araga, Katsuya Kikuchi, Masahiro Aoyagi
National Institute of Advanced Industrial Science and Technology (AIST), Japan

VIII-19 Electrical Interconnect Test Method of 3D ICs by Injected Charge Volume

Daisuke Suga[1], Masaki Hashizume[1], Hiroyuki Yotsuyanagi[1], Shyue-Kung Lu[2]
[1]Institute of Technology and Science, Tokushima University, Japan, [2]National Taiwan University of Science and Technology, Taiwan

VIII-20 Improved Access Pattern for ROB soft error rate Mitigation based on 3D Integration Technology

Chao Song, Minxuan Zhang
College of Computer, National University of Defense Technology, China

VIII-21 Best Engineering Practice for Thermal Characterization of Stacked Dice FPGA Devices

Arun Raghupathy[1], Hoa Do[2], Brian Philofsky[2], Gamal Refai-Ahmed[2]
[1]Electronic Cooling Solutions Inc, USA, [2]Xilinx Inc, USA

VIII-22 Electrical Interconnect Test of 3D ICs made of Dies without ESD Protection Circuits with a Built-in Test Circuit

Kosuke Nanbara[1], Akihiro Odoriba[1], Masaki Hashizume[1], Hiroyuki Yotsuyanagi[1], Shyue-Kung Lu[2]
[1]Institute of Technology and Science, Tokushima University, Japan, [2]National Taiwan University of Science and Technology, Taiwan

VIII-23 Congestion-Aware Optimal Techniques for Assigning Inter-Tier Signals to 3D-Vias in a 3DIC

Gopi Neela, Jeffrey Draper
Information Sciences Institute, University of Southern California, USA

VIII-24 On TSV Array Defect Detection Method Using Two Ring-oscillators Considering Signal Transitions at Adjacent TSVs

Hiroyuki Yotsuyanagi, Akihiro Fujiwara, Masaki Hashizume
Institute of Technology and Science, Tokushima University, Japan

VIII-25 Crosstalk-Included Eye-Diagram Estimation for High-speed Silicon, Organic, and Glass Interposer Channels on 2.5D/3D IC

Sumin Choi[1], Heegon Kim[1], Daniel H. Jung[1], Jonghoon J. Kim[1], Jaemin Lim[1], Hyunsuk Lee[1], Kyungjun Cho[1], Joungho Kim[1], Hyungsoo Kim[2], Yongju Kim[2], Yunsaing Kim[2]
[1]Department of Electrical Engineering, TERA Lab, Korea Advanced Institute of Science and Technology, Daejeon, South Korea, [2]Design Technology Group, SK Hynix Inc., Icheon, Gyeonggi-do, South Korea

VIII-26 Consideration of Microbump Layout for Reduction of Local Bending Stress Due to CTE Mismatch in 3D IC

Hisashi Kino[1], Hideto Hashiguchi[2], Seiya Tanikawa[2], Yohei Sugawara[2], Shunsuke Ikegaya[3], Takafumi Fukushima[2, 4], Mitsumasa Koyanagi[4], Tetsu Tanaka[2, 3]
[1]Frontier Research Institute for Interdisciplinary Sciences (FRIS), Tohoku University, Japan, [2]Dept. of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University, Japan, [3]Dept. of Biomedical Engineering, Graduate School of Biomedical Engineering, Tohoku University, Japan, [4]New Industry Creation Hatchery Center (NICHe), Tohoku University, Japan

Sep. 1 (Tue)

VIII-27 Characterization of the Mechanical Stress Impact on Device Electrical Performance in the CMOS and III-V HEMT/HBT Heterogeneous Integration Environment

Eric J. Wyers[1], T. Robert Harris[2], W. Shep Pitts[2], Jordan E. Massad[3], Paul D. Franzon[2]
[1]Department of Engineering and Computer Science, Tarleton State University, Stephenville, TX, USA, [2]Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, USA, [3]Component Science and Mechanics Department, Sandia National Laboratories, Albuquerque, NM, USA

VIII-28 Design of a 3-D Stacked Floating-point Goldschmidt Divider

Jubee Tada[1], Ryusuke Egawa[2], Hiroaki Kobayashi[2]
[1]Graduate School of Science and Engineering, Yamagata University, Japan, [2]Research Division on Supercomputing Systems, Cyberscience Center, Tohoku University, Japan

VIII-29 Modeling and Analysis of Defects in Through Silicon Via Channel for Non-invasive Fault Isolation

Daniel H. Jung[1], Heegon Kim[1], Jonghoon J. Kim[1], Sukjin Kim[1], Hyun-Cheol Bae[2], Kwang-Seong Choi[2], Joungho Kim[1]
[1]Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, South Korea, [2]IT Materials and Components Laboratory, Electronics and Telecommunications Research Institute, Korea

VIII-30 Investigation of Effects of Metalization on Heat Spreading in Bump-bonded 3D Systems

Samson Melamed, Katsuya Kikuchi, Masahiro Aoyagi
National Institute of Advanced Industrial Science and Technology (AIST), Japan

VIII-31 Enabling Automatic System Design Optimization through Assembly Design Kits

Andy Heinig, Robert Fischbach
Fraunhofer IIS/EAS, Germany

VIII-32 Cost Modeling and Analysis for the Design, Manufacturing and Test of 3D-ICs

Armin Gruenewald, Michael G. Wahl, Rainer Brueck
Institute of Microsystem Engineering, University of Siegen, Germany

VIII-33 Proposed Static Timing Analysis Framework for Extracted 3D Integrated Circuits (3D-STA)

Mohamed N. ElBahey, DiaaEldin S. Khalil, Hani F. Ragai
ECE Department, Ain Shams University, Egypt

VIII-34 Noise Coupling Modeling and Analysis of Through Glass Via(TGV)

Insu Hwang[1], Jihye Kim[1], Youngwoo Kim[1], Jonghyun Cho[1], Venky Sundaram[2], Rao Tummala[2], Joungho Kim[1]
[1]Tera Lab, KAIST, Korea, [2]Packaging Research Center, Georgia Institute of Technology, USA

VIII-35 TSV Noise Coupling in 3D IC Using Guard Ring

R Ranga Reddy[1], Sugandh Tanna[1], Dr. Shiv Govind Singh[1], Om Krishna Singh[2]
[1]Department of Electrical Engineering, Indian Institute of Technology Hyderabad, India, [2]Department of Electronics & Information Technology (DeitY), Govt. of India

VIII-36 Power Tile Optimization and Packaging for efficient temperature Management of ASIC's in Networking applications

Susheela Narasimhan
Senior Staff Engineer, Juniper Networks Inc., Sunnyvale, CA, USA

Sep. 1 (Tue)

Room: Tachibana Conference Hall **16:35 – 17:40**

Technical Session (IX) <3D Imager and Device>

IX-1 **Invited Talk: Technology and Overview of Sony's 3D Stacked CMOS Image Sensor**

Tomoharu Ogita

Development Department 3, Imaging Device Development Division, Device & Material R&D Group, RDS Platform, Sony Corporation, Japan

IX-2 **Three-dimensional Integrated Circuits and Stacked CMOS Image Sensors Using Direct Bonding of SOI Layers**

Masahide Goto[1], Kei Hagiwara[1], Yoshinori Iguchi[1], Hiroshi Ohtake[1], Takuya Saraya[2], Masaharu Kobayashi[2], Eiji Higurashi[2], Hiroshi Toshiyoshi[2], Toshiro Hiramoto[2]

[1]NHK Science and Technology Research Laboratories, Japan, [2]The University of Tokyo, Japan

IX-3 **Fine-Grained 3-D Integrated Circuit Fabric Using Vertical Nanowires**

Mostafizur Rahman[1], Santosh Khasanvis[2], Jiajun Shi[2], Mingyu Li[2], Csaba Andras Moritz[2]

[1]Computer Science and Electrical Engineering, University of Missouri-Kansas City, United States, [2]Electrical and Computer Engineering, University of Massachusetts Amherst, United States

Room: Tachibana Conference Hall **18:00 – 19:30**

Rump Session (Wine & Cheese)

"Monolithic 3D vs. Multilithic 3D"

Moderator: Paul Franzon *(North Carolina State University, USA)*

Panelist: Sung Kyu Lim *(Georgia Tech, USA)*
Kazuyuki Higashi *(Toshiba, Japan)*
Toshifumi Irisawa *(AIST, Japan)*
Subramanian Iyer *(UCLA, USA)*
Paul Enquist *(Ziptronix, USA)*
Yasumitsu Orii *(IBM, Japan)*

Sep. 2 (Wed)

Sendai International Center **8:00 –**

Registration

Room: Tachibana Conference Hall **8:30 – 9:15**

Keynote (III)

Neuromorphic Semiconductor Memory

Chung H. Lam
IBM Research, USA

Room: Tachibana Conference Hall **9:15 – 10:40**

Technical Session (X) <3D Thermal Issues>

X-1 Invited Talk: A Holistic View of Chip-Level Thermal Architecture from Heterogeneous Stacked Dice to System Level in Telecoms Applications

Gamal Refai-Ahmed, Ivor Barber, Anthony Torza, Brian Philofsky
Xilinx, USA

X-2 Thermal Simulation of Heterogeneous GaN/InP/Silicon 3DIC Stacks

T. Robert Harris[1], Eric J. Wyers[2], Lee Wang[3], Samuel Graham[4], Georges Pavlidis[4], Paul D. Franzon[1], W. Rhett Davis[1]
[1]Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, USA, [2]Department of Engineering and Computer Science, Tarleton State University, Stephenville, TX, USA, [3]Calibre Design Solutions, Mentor Graphics Corporation, Fremont, CA, USA, [4]Department of Mechanical Engineering, Georgia Institute of Technology, Atlanta, GA, USA

X-3 Temperature-Aware Online Testing of Power-Delivery TSVs

Hua-Cheng Fu[1], Shi-Yu Huang[1], Ding-Ming Kwai[2], Yung-Fa Chou[2]
[1]Electrical Engineering Dept., National Tsing Hua University, Taiwan, [2]ICL, Industrial Technology Research Institute, Taiwan

X-4 Graphite-based Heat Spreaders for Hotspot Mitigation in 3D ICs

Cristiano Santos[1], Rafael Prieto[2], Pascal Vivet[1], Jean-Philippe Colonna[1], Perceval Coudrain[2], Ricardo Reis[3]
[1]CEA-Leti, France, [2]STMicroelectronics, France, [3]PGMICRO-UFRGS, Brazil

Break (10:40 – 10:55)

Sep. 2 (Wed)

Room: Tachibana Conference Hall 10:55 – 12:20

Technical Session (XI) <Interposer Technologies>

XI-1 **Invited Talk: Active Si Interposer for 3D IC Integrations**

Joungho Kim
Korea Advanced Institute of Science and Technology, Korea

XI-2 **Processing Active Devices on Si Interposer and Impact on Cost**

Dimitrios Velenis, Mikael Detalle, Geert Hellings, Mirko Scholz, Erik Jan Marinissen, Geert Van der Plas, Antonio La Manna, Andy Miller, Dimitri Linten, Eric Beyne
IMEC, Belgium

XI-3 **Silicon Interposer Platform With Low-Loss Through-Silicon Vias Using Air**

Hanju Oh, Gary S May, Muhannad S Bakir
School of Electrical and Computer Engineering, Georgia Institute of Technology, USA

XI-4 **Stress Management Strategy to Limit Die Curvature During Silicon Interposer Integration**

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Room: Tachibana Conference Hall 12:20 – 12:30

Closing Remark

(Lunch)

13:30 – 17:30

Social Program <GINTI Tour>