IEEE 3D System Integration Conference 2014

Technical Program

December 1-3 2014, Actons Hotel, Kinsale, Cork, Ireland

Sunday, November 30th

19:00-20:00 Conference Registration

20:00 Whiskey tasting and talk by the Irish Whiskey Society

Monday, December 1st

08:00 – 09:00 Conference Registration

09:00 - 09:10 Opening Address – Kieran F Drain, CEO, Tyndall National Institute

09:10 - 09:30 Invited Talk 1 – "Trends in 3DIC", Thibault Buisson, Yole

09:30 - 10:10 Invited Talk 2 – "3D System Design: opportunities, challenges, enabling solutions and methodologies" Denis Dutoit, CEA-Leti

10:10 - 11:00 Session 1 3DIC

- **O1 -** Dorota S. Temple, Dean Malta, Erik P. Vick, Matthew R. Lueck, Scott H. Goodwin, Mark S. Muzilla, Christopher M. Masterjohn and Mark R. Skokan "Advanced 3D mixed-signal processor for infrared focal plane arrays: fabrication and test"
- **O2** - Paul D. Franzon, Eric Rotenberg, James Tuck, Huiyang Zhou, W. Rhett Davis, Hongwen Dai, Joonmoo Huh, Sunkgwan Ku, Steve Lipa, Chao Li, Jong Beom Park, Joshua Schabel "3D-Enabled Customizable Embedded Computer (3DECC)"

11:00 - 11:20 Break

11:20 - 13:00 Session II 2.5/3D Processing

- **O3** - Naoya Watanabe, Masahiro Aoyagi, Daisuke Katagawa, Tsubasa Bandoh, Takahiko Mitsui and Eiichi Yamamoto "Small-Diameter TSV Reveal Process Using Direct Si/Cu Grinding and Metal Contamination Removal"
- **O4** - Takafumi Fukushima, Yuka Ito, Murugesan Mariappan, Jiceol Bea, Kangwook Lee, Koji Choki, Tetsu Tanaka and Mitsumasa Koyanagi "Tiny VCSEL Chip Self-Assembly for Advanced Chip-to-Wafer 3D and Hetero Integration"

- **O5** - Joeri De Vos, Vladimir Cherman, Mikael Detalle, Teng Wang, Abdellah Salahouelhadj, Robert Daily, Geert Van der Plas and Eric Beyne “Comparative study of 3D stacked IC and 3D interposer integration: processing and assembly challenges.”
- **O6** - Fumihiro Inoue, Harold Philipsen, Marleen van der Veen, Kevin Vandersmissen, Stefaan Van Huylenbroeck, Herbert Struyf and Tetsu Tanaka “Cu Seeding Using Electroless Deposition on Ru Liner for High Aspect Ratio Through-Si Vias”

13:00 - 14:00 Lunch

14:00 - 14:40 Invited Talk 3 – “Recent innovations in FPGA silicon and packaging technology”
Brendan Farley, Xilinx

14:40 - 16:00 Session III Electrical Design

- **O7** - Masaki Hashizume, Shoichi Umezu, Hiroyuki Yotsuyanagi and Shyue-Kung Lu “A Built-in Supply Current Test Circuit for Electrical Interconnect Tests of 3D ICs”
- **O8** - Sonda Chtourou, Vinod Pangracious, Emna Amouri, Zied Marrakchi, Habib Mehrez and Mohamed Abid “Three-dimensional Mesh of Clusters: An Alternative Unified High Performance Interconnect Architecture for 3D-FPGA Implementation”
- **09** - Robert Fischbach, Andy Heinig and Peter Schneider “Design Rule Check and Layout Versus Schematic for 3D Integration and Advanced Packaging”

16:00 - 16:30 Break

16:30 – 17:45 Session IV Test

- **O10** - Yann Beilliard, Stéphane Moreau, Léa Di Cioccio, Perceval Coudrain, Giovanni Romano, Antoine Nowodzinski, F. Aussenac, Pierre-Henri Jouneau, Emmanuel Rolland and Thomas Signamarcheix “Advances Toward Reliable High Density Cu-Cu Interconnects by Cu-SiO2 Direct Hybrid Bonding”
- **O11** - Jonghoon J. Kim, Bumhee Bae, Sukjin Kim, Sunkyu Kong, Heegon Kim, Daniel H. Jung and Joungho Kim “Magnetically-Coupled Current Probing Structure Consisting of TSVs and RDLs in 2.5D and 3D-IC”
- **O12** - Khadim Dieng, Philippe Artillan, Cédric Bermond, Olivier Guiller, Thierry Lacrevaz, Sylvain Joblot, Grégory Houzet, Alexis Farcy, Yann Lamy and Bernard Fléchet “Electrical Model and Characterization of Through Silicon Capacitors (TSC) in Silicon Interposer”

18:00 Historical Walking Tour of Kinsale

19:00 – 21:00 **Poster Session**

All posters and authors will be available

Tuesday, December 2nd

08:00 – 09:00 Conference Registration

09:00 – 09:40 Invited Talk 4 – “Design for 3D – the way from specification to a verified system”
Peter Schneider, Fraunhofer Institute for Integrated Circuits

09:40 – 10:55 Session V 2.5/3D Processing II

- **O13** - Kangwook Lee, C.Nagai, Ai Nakamura, Jichel Bea, Maripan Murugesan, Takafumi Fukushima, Tetsu Tanaka and Mitsumasa Koyanagi “Effects of Electro-less Ni Layer as Barrier/Seed Layers for High Reliable and Low Cost Cu TSV”
- **O14 -** Jing Tao, Alan Mathewson and Kafil M. Razeeb “Bumpless Interconnects formed with Nanowire ACF for 3D Applications”
- **O15** - Oded Raz, Pinxiang Duan and Harmen J.S. Dorren “Simple and Low Cost Technique for Stacking Known Good Dies to Create Compact 3D Stacked Parallel Optics Assemblies”

10:55 - 11:20 Break

11:20 - 12:10 Session VI RF

- **O16** - Xiao Sun, Geert Van der Plas, Mikael Detalle and Eric Beyne “Analysis of 3D interconnect performance: effect of the Si substrate resistivity”
- **O17** - Katsuya Kikuchi, Masaaki Ujiie, Masahiro Aoyagi and Shinya Takayama “Ultrawideband Ultralow PDN Impedence of Decoupling Capacitor Embedded Interposers Using Narrow Gap Chip Parts Mounting Technology for 3-D Integrated LSI System”

12:10 - 12:50 Invited Talk 5 – “EUROSERVER: Riding the perfect storm” John Goodacre, ARM

12:50 - 13:45 Lunch

13:45 - 14:35 Session VII Metrology

- **O18** - Mariappan Murugesan, Yasuhiko Imai, Shigeru Kimura, Takafumi Fukushima, Jichel Bea, Kangwook Lee, Tetsu Tanaka and Mitsumasa Koyanagi “Micro-XRD Investigation of Fine-Pitch Cu-TSV Induced Thermo-Mechanical Stress in High-Density 3D-LSI”
- **O19** - Emma Kowalczuk, Arnab Bhattacharya, Ka Chung Lee, Jesse Alton, Martin Igarashi and Stephane Barbeau “Fault Localisation of defects using Electro Optical Terahertz Pulse Reflectometry and 3D EM modelling with Virtual Known Good Device”

14:35 – 15:50 Session XI Thermal Issues

- **O20** - Cristiano Santos, Pascal Vivet, Jean-Philippe Colonna, Perceval Coudrain and Ricardo Reis “Thermal Performance of 3D ICs: Analysis and Alternatives”
- **O21** - Keiji Matsumoto, Hiroyuki Mori, Tasumitsu Orii “Cooling from the bottom side (laminate (substrate) side) of a three-dimensional (3D) chip stack”

- **O22** - Cristiano Santos, Papa Momar Souare, Perceval Coudrain, Jean-Philippe Colonna, François de Crécy, Pascal Vivet, Andras Borbely, Ricardo Reis, Haykel Ben Jamaa, Vincent Fiori and Alexis Farcy “Using TSVs for Thermal Mitigation in 3D Circuits: Wish and Truth”

15:50 - 16:05 Break

16:05 – 17:45 Session VIII 2.5/3D Processing III

- **O23** - Pascal Couderc, Renzo Dalmolin and Jerome Noiray “Application of WDoD™ technology for the manufacturing of a leadless pacemaker”
- **O24** - Mehdi Saeidi, Kambiz Samadi, Arpit Mittal and Rajat Mittal “Thermal Implications of Mobile 3D-ICs”
- **O25** - Yoriko Mizushima, Youngsuk Kim, Tomoji Nakamura, Shoichi Kodama, Nobuhide Maeda, Koji Fujimoto and Takayuki Ohba “Impact of Thermomechanical Stresses on Ultra-thin Si stacked structure”
- **O26** - Tung T. Bui, Xiaojin Cheng, Naoya Watanabe, Fumiki Kato, Katsuya Kikuchi and Masahiro Aoyagi “Copper Filled TSV Formation with Parylene-HT Insulator for Low-Temperature Compatible 3D Integration”

19:30 Gala Dinner

Wednesday, December 3rd

09:00 – 09:40 Invited Talk 6 – “Controlling Thermal Processing to Enable a 3D World” Patrick Martin, Applied Materials

09:40 – 10:55 Session X 2.5/3D Processing IV/ Thermal

- **O27** - Chaoqi Zhang, Hyung Suk Yang and Muhannad S. Bakir “Au-NiW Mechanically Flexible Interconnects (MFIs) for Rematable 3D Integration”
- **O28** - Severin Zimmermann, Thomas Brunschwiler, Guo Hong, Jonas Zuercher, Brian Burg, Mario Baum, Christian Hofmann and Dimos Poulikakos “Characterization of particle beds in percolating thermal underfills based on centrifugation”
- **O29** - Yasuhiro Morikawa, Takahide Murayama and Toshiyuki Sakuishi “TSV Etching Process Integration for High Reliability.”

10:55 - 11:10 Break

11:10 - 11:45 Invited Talk 7 – Nanowire based Anisotropic Conductive Film for 3D integration, Kafil M. Razeeb, Tyndall

11:45 – 12:15 Prize giving and closing of Conference

12:15 Bus to Tyndall

13:30 – 17:30 CST Workshop/Tour of Tyndall

Posters

P1 Analysis of Thermal Stress Distribution for TSV with Novel Structure, Wei Feng, Naoya Watanabe, Haruo Shimamoto, Katsuya Kikuchi and Masahiro Aoyagi

P2 Conventional magnetron sputtering of metal seed layers on high aspect ratio vias with tilting, Young Sik Song, Yunho Han and Tai Hong Yim

P3 Fault Detection and Isolation of Multiple Defects in Through Silicon Via (TSV) Channel, Daniel Jung, Heegon Kim, Jonghoon Kim, Sukjin Kim, Kwang-Seong Choi, Hyun-Cheol Bae and Joungho Kim

P4 Manufacturing and Test Assistance for 3D-Integrated Heterogeneous Systems, Armin Gruenewald, Michael Wahl and Rainer Brueck

P5 Leveraging 3D-IC for On-chip Timing Uncertainty Measurements, Randy Widialaksono, Wenxu Zhao, William Rhett Davis and Paul D. Franzon

P6 On-Chip Checkpointing with 3D-Stacked Memories, Masayuki Sato, Ryusuke Egawa, Hiroyuki Takizawa and Hiroaki Kobayashi

P7 Thermal Challenges for Heterogeneous 3D ICs and Oppurtunities for Air Gap Thermal Isolation, Yang Zhang, Thomas Sarvey and Muhannad Bakir

P8 Electroless metal deposition for IC and TSV applications, James Rohan, Declan Casey, Monika Zygowska, Michael Moore and Brian Shanahan

P9 A Cost Benefit Analysis: the Impact of Defect Clustering on the Necessity of Pre-bond Tests, Qiaosha Zou, Matt Poremba and Yuan Xie

P10 Metal coated polymer spheres for compliant fine pitch ball grid arrays, Daniel Nilsen Wright, Astrid-Sofie Borge Vardøy, Maaike Margrethe Visser Taklo and Helge Kristiansen

P11 An Impact of Circuit Scale on the Performance of 3-D Stacked Arithmetic Units, Jubee Tada, Ryusuke Egawa and Hiroaki Kobayashi

P12 Modeling of Substrate Contacts in TSV-based 3D ICs, Masayuki Watanabe, Masa-Aki Fukase, Masashi Imai, Nanako Niioka, Tetsuya Kobayashi, Rosely Karel and Atsushi Kurokawa

P13 Substrate Monitoring System for Inspecting Defects in TSV-Based Data Bus, Yuuki Araga, Katsuya Kikuchi and Masahiro Aoyagi

P14 Analysis and Optimization of a Power Distribution Network in 2.5D IC with Glass Interposer, Youngwoo Kim, Jonghyun Cho, Kiyeong Kim, Joungho Kim, Rao Tummala, Venky Sundaram and Srikrishna Sitaraman

P15 Innovative SiC over Si photodiode based dual-band, 3D Integrated detector, Andrzej Kociubinski, Mariusz Duk, Tomasz Bieniek, Grzegorz Janczyk and Michal Borecki

P16 Thermal effects of heterogeneous interconnects on InP / GaN / Si diverse integrated circuits. T Robert Harris, Lee Wang, Paul Franzon and W Rhett Davis

P17 Advanced Processing for High Efficiency Inductors for 2.5D/3D Power Supply in Package, Ricky Anthony, Santosh Kulkarni, Ningning Wang and Cian Ó Mathúna

P18 Novel Methodology for 3D MEMS-IC Design and Co-simulation on MEMS Microphone Smart System Example, Tomasz Bieniek, Grzegorz Janczyk, Magdalena Ekwińska and Andrzej Kociubiński

P19 An Impact of Circuit Scale on the Performance of 3-D Stacked Arithmetic Units, Jubee Tada, Ryusuke Egawa and Hiroaki Kobayashi

P20 Designing Vertical Bandwidth Reconfigurable 3D NoCs for Many Core Systems, Qiaosha Zou, Jia Zhan, Fen Ge and Yuan Xie

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