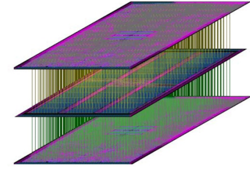
IEEE 3D System Integration Conference 2013

Technical Program

October 2-4, 2013, San Francisco, California, USA



Wednesday, October 2nd

09:00 – 12:00 IARPA Workshop **Metropolitan II**

Title: IARPA 3D Technology Forum

Description: *The Intelligence Advanced Research Projects Agency (IARPA) is a sponsor of external research and development programs to advance the state-of-the-art in compelling technologies. This forum will focus on the latest results of IARPA's program to advance 3D heterogeneous integration using innovative silicon manufacturing base technologies. This forum features a panel with presentations from the program's performers that are exploring materials and 3D device integration on silicon for exemplary applications in communications, signal processing, and sensing.*

--Free and open to all 3DIC attendees--

13.00 – 18:00 Tutorials **Metropolitan II**

13.00 – 15.00 "Design for 3DIC", Prof. Franzon - NCSU

15.00 – 16.00 "ASET's 3DIC Learning Experience", Prof. Koyanagi, Tohoku University

16.00 – 17.00 "TSV and Interposer Design for High Perform. and Low Noise ", Prof. Kim - Kaist

17.00 – 18.00 "Monolithic 3DIC", Zvi Or-Bach

18:30 – 20:00 Welcome Reception **Metropolitan III**

Thursday, October 3rd

8:00 – 9:00 Continental Breakfast **Metropolitan Foyer**

09:00 – 09:05 Welcome: Conference Chairs **Metropolitan II**

09:05 – 09:50 Keynote: Session Chair – Paul Franzon – NC State **Metropolitan II**

Title: "European Activities in Heterogeneous Sensor Integration (e-BRAINS)"

Author: Maaike M. Visser Taklo, PhD, Research Manager at SINTEF ICT, Norway

09:50 – 10:20 Invited Talk I **Metropolitan II**

Title: "3DIC Activity at Tohoku Univ."

Author: Prof. Mitsu Koyanagi, Tohoku University

10:20 – 10:45 Break **Metropolitan Foyer**

10:45 – 12:00 Session I 3DIC : Session Chair – Dr. Rozalia Beica, Yole **Metropolitan II**

- Kangwook Lee, Seiya Tanikawa, Mariappine Murugesan, Jicheol Bea, Hideki Naganuma, Takafumi Fukushima, Tetsu Tanaka, and Mitsumasa Koyanagi, "Impact of 3-D integration process on memory retention characteristics in thinned DRAM chip for 3-D memory", New Industry Creation Hatchery Center (NICHe), Tohoku University, Sendai, Japan
- Paul Franzon, Avi-Bar Cohen "Thermal Requirements in Future 3D Processors", North Carolina State University, Raleigh, NC, USA, DARPA, Arlington VA, USA
- Qiuling Zhu, Berkin Akin, H. Ekin Sumbul, James C. Hoe, Larry Pileggi, Franz Franchetti, "A 3D-Stacked Logic-in-Memory Accelerator for Application-Specific Data Intensive Computing", Carnegie Mellon University, Pittsburgh, PA, USA

12:00 – 13:00 Lunch **Metropolitan III**

13:00 – 13:30 Invited Talk II : Session Chair – Dr. Phil Garrou, Microelectronic Consultants of NC

Title: "A Perspective on Manufacturing 2.5/3D" **Metropolitan II**

Author: Dr. Robert Patti, Tezzaron

13:30 – 14:45 Session II 2.5/3D Processing I : Session Chair –Dr. Peter Ramm, Fraunhoffer SMFT

Metropolitan I

- M. Lueck, C. Gregory, A. Huffman, D. Malta, J. Lannon, D. S. Temple, "High Density Interconnect Bonding of Heterogeneous Materials using Non-Collapsible Microbumps at 10 µm pitch", Center for Materials and Electronics Technologies, RTI Int., Research Triangle Park, NC
- T. Nakamura, Y. Mizushima, H.Kitada, Y. S. Kim, N. Maeda, S. Kodama, A. Kawai, R.Sugie, H. Hashimoto, A. Uedono, K. Arai, and T. Ohba, "Influence of wafer thinning process on backside damage in 3D integration", Fujitsu Laboratories Ltd., Kanagawa, Japan, Tokyo Institute of Technology, Kanagawa, Japan, The University of Tokyo, Tokyo, Japan, DISCO Corp, Tokyo, Japan; Toray Research Center, Shiga, Japan, and University of Tsukuba, Ibaraki, Japan
- Yann Civale, Ranjith Samuel E. John, Herman Meynen, PengFei Fu, Craig Yeakle, Sheng Wang, Stefan Krausse, Thomas Rapps, and Stefan Lutter, "Cost-effective Temporary Bonding and Debonding Material Solution Towards High-Volume Manufacturing 2.5D/3D Through-Silicon Via Integrated Circuits", Dow Corning Europe, Seneffe, Belgium, Dow Corning Corporation, Midland, MI, USA, and Suss MicroTec, Sternenfels, Germany

13:30 – 14:45 Session III Electrical Design : Session Chair – Rhett Davis, NC State **Metropolitan II**

- Satoshi Takaya, Makoto Nagata, and Hiroaki Ikeda*,"Very low-voltage swing while high-bandwidth data transmission through 4096 bit TSV", Kobe University, Japan, and *ASET, Japan
- Jonghyun Cho, Youngwoo Kim, Venky Sundaram, Rao Tummala, and Joungho Kim, "Analysis of Glass Interposer PDN and Proposal of PDN Resonance Suppression Method" Georgia Institute of Technology, Atlanta GA.
- Heegon Kim, Jonghyun Cho, Jonghoon J. Kim, Daniel H. Jung, Sumin Choi, Junho Lee, Kunwoo Park, and Joungho Kim, "Eye-diagram Simulation and Analysis of a High-speed TSV-based Channel", Terahertz Interconnection and Package Laboratory, KAIST, Korea, and Advanced Design Team, SK Hynix Semiconductor, Korea

14:45 – 15:15 Break **Metropolitan Foyer**

15:15 – 17:00 Session IV 2.5 / 3D Processing II: Session Chair - Prof. Mitsu Koyanagi, Tohoku Univ.

Metropolitan I

- Yan-Pin Huang, Ruoh-Ning Tzeng, Yu-San Chien, Ming-Shaw Shy, Teu-Hua Lin, Kou-Hua Chen, Ching-Te Chuang, Wei Hwang, Chi-Tsung Chiu, Ho-Ming Tong, and Kuan-Neng Chen "Low Temperature (< 180°C) Bonding for 3D Integration", Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, and ASE, Kaohsiung, Taiwan

- S. Joblot, A. Jouve, M. Argoud, A. Garnier, F. de Crécy, C. Ferrandon, J.P. Colonna, R. Franiatte, C. Laviron, and S. Cheramy, "Wafer level encapsulated materials evaluation for chip on wafer (CoW) approach in 2.5D Si interposer integration", STMicroelectronics, Crolles, France, and CEA-LETI, MINATEC, Grenoble, France
- Osamu Nukaga, Tatsuya Shioiri, Satoshi Yamamoto, and Tatsuo Suemasu, "Glass Interposer with High-Density Three-Dimensional Structured TGV for 3D Systems Integration", Fujikura Ltd., Chiba, Japan

15:15 – 17:00 Session V Test : Session Chair Dr. Robert Patti, Tezzaron **Metropolitan II**

- Mottaqiallah Taouil, Said Hamdioui, Erik Jan Marinissen, and Sudipta Bhawmik, "Using 3D-COSTAR for 2.5D Test Cost Optimization", Delft Univ., Delft, Netherlands; IMEC Leuven, Belgium, and Qualcomm, Bridgewater, NJ, USA
- James Quinn, and Barbara Loferer, "Quality in 3D Assembly – Is "Known God Die" Good Enough?", Multitest, Rosenheim, Germany
- Shreepad Panth, Kambiz Samadi, and Sung Kyu Lim, "Test-TSV Estimation During 3D-IC Partitioning", Georgia Institute of Technology, Atlanta, GA, and Qualcomm Research, San Diego, CA

17:00 – 18:00 Panel Session **Metropolitan II**

Title: "The Progress and Remaining Obstacles to 3D ICs and 2.5D HVM"

Moderator: *E. Jan Vardaman*, TechSearch International

Panel Members: *Mitsumasa Koyanagi*, Professor & CTO, Dept. of Bioengineering and Robotics, Advanced Bio-Nano Devices Lab, Tohoku University

Dimitrios Velenis, Researcher, Integration Cost Analysis and Modeling Specialist, 3D Technologies, Process Technology Unit, IMEC

Tom Gregorich, Director, Package Engineering, Broadcom

Doug Anberg, Director of Marketing, Ultratech

Dongkai Shangguan, Founding CEO, National Center for Advanvced Packaging (NCAP China)

18:00 – 19:30 Poster Session **Metropolitan III**

All posters and authors will be available

19:30 – 21:00 Banquet **Ducca Patio**

Friday, October 4th

08:00 – 09:00 Continental Breakfast **Metropolitan Foyer**

09:00 – 09:30 Invited talk III : Session Chair – Dr. Phil Garrou, Microelectronic Consultants of NC

Title: "The DARPA ICECool Program" **Metropolitan II**

Author: Avi Bar-Cohen, DARPA

09:45 – 10:35 Session VI Integrated Antenna: Session Chair – Dr MMV Talko, SINTEF **Metropolitan I**

- Julia Hsin-Lin Lu, Wing-Fai Loke, Dimitrios Peroulis, and Byunghoo Jung, "Implementing Wireless Communication Links in 3-D ICs Utilizing Wide-Band On-Chip Meandering Microbump Antenna", School of Electrical and Computer Engineering, Purdue University, USA

- Y. Lamy, O. El Bouayadi, C. Ferrandon, L. Dussopt, A. Siligaris, C.Dehos, and P. Vincent, "A compact 3D silicon interposer package with integrated antenna for 60GHz wireless applications", CEA- LETI, Grenoble, France

09:45 – 10:35 Session VII 2.5/3D Processing III : Session Chair - Dr. Matt Lueck, RTI Int

Metropolitan II

- Bipin Rajendran, Albert K. Henning, Brian Cronquist, and Zvi Or-Bach, "Pulsed Laser Annealing: A scalable and practical technology for monolithic 3D IC", Dept. of Electrical Engineering, IIT Bombay, India, and MonolithIC 3D Inc, San Jose, CA
- René Puschmann, Mathias Boettcher, Irene Bartusseck, Frank Windrich, Conny Fiedler, Peggy John, Charles Manier, Kai Zoschke, Jürgen Grafe, Hermann Oppermann, M. Jürgen Wolf, K. Dieter Lang, and Michael Ziesmann, "3D Integration of standard integrated circuits", Fraunhofer IZM ASSID, and NXP Semiconductors Germany Hamburg, Germany

10:35 – 10:50 Break **Metropolitan Foyer**

10:50 – 12:05 Session VIII RF and 3D: Session Chair – Dr Paul Enquist, Ziptronix **Metropolitan I**

- M. Brocard, C. Bermond, T. Lacrevaz, A. Farcy, P. Le Maître, P. Scheer, P. Leduc, S. Chéramy, and B. Fléchet, "RF Characterization of substrate coupling between TSV and MOS transistors in 3D integrated circuits", STMicroelectronics, Crolles, France, IMEP-LAHC; Université de Savoie Cedex, France, and CEA- LETI, Grenoble, FR
- Tiantao Lu, and Ankur Srivastava, "Detailed Electrical and Reliability Study on Tapered TSVs" University of Maryland, College Park, MD
- Thorbjörn Ebefors, „Jessica Fredlund, Daniel Perttu, Raymond van Dijk, Lorenzo Cifola, Mikko Kaunisto, Pekka Rantakari, and Tauno Vähä-Heikkilä, "The Development and Evaluation of RF TSV for 3D IPD Applications", Silex Microsystems AB, Järfälla, Sweden

10:55 – 12:05 Session IX Applications & Metrology : Session Chair – Dr Larry Smith, Sematech

Metropolitan II

- Valerio Re, Massimo Manghisoni, Gianluca Traversi, Luigi Gaioni, Alessia Manazza, and Lodovico Ratti, "Active pixel sensors with enhanced pixel-level analog and digital functionalities in a 2-tier 3D CMOS technology", Università di Bergamo, Dalmine, Italy; Università di Pavia, Pavia, Italy, and INFN, Pavia, Italy
- Vinod Pangracious, Habib Mehrez, and Zied Marakchi, "Designing a 3D Tree-based FPGA: Optimization of Butterfly Programmable Interconnect Topology Using 3D Technology", University of Pierre and Marie Curie, Paris, France, and FlexRas Technologies, Paris, France
- Yuri Sylvester, Sr. Semiconductor Technologist, "3D X-Ray Microscopy: A Near-SEM Non-Destructive Imaging Technology Used in the Development of 3D IC Packaging", Xradia, Inc

12:05 – 13:15 Lunch **Metropolitan III**

13:15 – 14:55 Session X Design Directions in 3DIC : Session Chair – Prof. Paul Franzon, NC State

Metropolitan I

- Erfan Azarkhish, Igor Loi, and Luca Benini,"A High-performance Multiported L2 Memory IP for Scalable Three-dimensional Integration", DEI, University of Bologna, Bologna, Italy
- Y. Lamy, J.P. Colonna, G. Simon, P. Leduc, S. Cheramy, and C. Laviron, "Which interconnects for which 3D applications? Status and perspectives", CEA- LETI, Grenoble, France
- Zhenqian Zhang, Brandon Noia, Krishnendu Chakrabarty, and Paul Franzon, "Face-to-face Bus Design with Built In Self-Test in 3D ICs", NC State Univ. Raleigh, NC and Duke University, Durham, NC
- Zhenqian Zhang and Paul Franzon, "TSV-based, Modular and Collision Detectable Face-to-back Shared Bus Design", NC State University, Raleigh, NC

13:15 – 14:55 Session XI 2.5/3D Processing IV : Session Chair - Jeff Burns, IBM **Metropolitan II**

- Dimitrios Velenis, Mikael Detalle, Erik Jan Marinissen, and Eric Beyne ,"Si Interposer Build-up Options and Impact on 3D System Cost", IMEC, Leuven, Belgium
- Yann Beilliard, Léa Di Cioccio, Perceval Coudrain, Stéphane Moreau, Loic Sanchez, Brigitte Montmayeul, Thomas Signamarcheix, Rafael Estevez, and Guillaume Parry, "Chip to wafer copper direct bonding electrical characterization and thermal cycling", CEA- LETI, Grenoble, France, CEA, LETI, MINATEC, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France, and, CNRS, Grenoble, France
- T. Fukushima, J. Bea, M. Murugesan, H.-Y. Son, M.-S. Suh, K.-Y. Byun, N.-S. Kim, K.-W. Lee, and M. Koyanagi, "3D Memory Chip Stacking by Multi-Layer Self-Assembly Technology", New Industry Creation Hatchery Center (NICHe), Tohoku University, Sendai, Japan and SK Hynix, Icheon, Korea
- Jason Chew, Uday Mahajan, Rajeev Bajaj, Iad Mirshad, Lucia Feng, and Robert Newcomb, "Characterization and Optimization of a TSV CMP Reveal Process using a Novel Wafer Inspection Technique for Detecting Sub-Monolayer Surface Contamination", Applied Materials, Singapore; Applied Materials, Santa Clara; Qcept Technologies, Atlanta, GA

14:55 – 15:15 Break **Metropolitan Foyer**

15:15 – 17:00 Session XII Thermal: Session Chair – Prof Avram Bar-Cohen, DARPA **Metropolitan I**

- Yassir Madhour, Michael Zervas, Gerd Schlottig, Thomas Brunschwiler, Yusuf Leblebici, John Richard Thome, and Bruno Michel, "Integration of intra chip stack fluidic cooling using thin-layer solder bonding", Heat and Mass Transfer Laboratory, Swiss Institute of Technology, Lausanne, Switzerland, and IBM Research , Zurich, Switzerland
- Yue Zhang, Hanju Oh, and Muhannad S. Bakir, "Within-Tier Cooling and Thermal Isolation Technologies for Heterogeneous 3D ICs", School of Electrical & Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA
- Benjamin Vianne, Pierre Bar, Vincent Fiori, Sébastien Petitdidier, Norbert Chevrier, Sébastien Gallois-Gareignot, Alexis Farcy, Pascal Chausse, Stéphanie Escoubas, Nicolas Hotellier, and Olivier Thomas, "Thermo-mechanical Study of a 2.5D Passive Silicon Interposer Technology: Experimental, Numerical and In-Situ Stress Sensors Developments", STMicroelectronics, Crolles France; STMicroelectronics, Grenoble, France; CEA-LETI, Grenoble, France, and Aix-Marseille Université, Marseille, France

15:15 – 17:00 Session XIII Redundancy, Design Planning : Session Chair – Prof Joungho Kim, KAIST

Metropolitan II

- Hiroyuki Hashimoto, Takafumi Fukushima, Kangwook Lee, Tetsu Tanaka, and Mitsumasa Koyanagi, "Highly Efficient TSV Repair Technology for Resilient 3-D Stacked Multicore Processor System" New Industry Creation Hatchery Center (NICHe), Tohoku University, Sendai, Japan, and Tohoku University, Sendai, Japan
- William Wahby, Ashish Dembla, and Muhannad Bakir, "Evaluation of 3DICs and Fabrication of Monolithic Interlayer Vias", Georgia Institute of Technology, Atlanta, GA
- Artur Quiring, Markus Olbrich, and Erich Barke, "Improving 3D-Floorplanning Using Smart Selection Operations in Meta-Heuristic Optimization", Institute of Microelectronic Systems, Leibniz Univ., Hannover, Germany
- Ryusuke Egawa, Masayuki Sato, Jubee Tada, and Hiroaki Kobayashi, "Vertically Integrated Processor and Memory Module Design for Vector Supercomputers", Cyberscience Center, Tohoku University, Yamagata University, and JST CREST

Posters

- Stephen H. Pan, Tadaaki Hitom, and Norman Chang, "3D-IC Dynamic Thermal Analysis with Hierarchical and Configurable Chip Thermal Model", Apache Design, Inc., San Jose, CA, USA,
- Cristiano Santos, Pascal Vivet, Denis Dutoit, Philippe Garrault, Nicolas Peltier, and Ricardo Reis, "System-Level Thermal Modeling for 3D Circuits: Characterization with a 65nm Memory-on-Logic Circuit", CEA-Leti, Grenoble, France, DOCEA Power Inc., Moirans, France, and UFRGS, Porto Alegre, Brazil
- Keiji Matsumoto, Soichiro Ibaraki, Kuniaki Sueoka, Katsuyuki Sakuma, Hidekazu Kikuchi, Hiroyuki Mori, Yasumitsu Orii, Fumiaki Yamada, Kohei Fujihara, Junichi Takamatsu, and Koji Kondo, "Thermal design guideline and new cooling solution for a three-dimensional (3D) chip stack", IBM Research-Tokyo, Japan; IBM Corp., Hopewell Jct, NY, Association of Super-Advanced Electronics Technologies(ASET), Tokyo, Japan and Denso Corporation , Aichi-ken, Japan
- Katsuya Kikuchi, Yotaro Yasu, Fumiki Kato, Shunsuke Nemoto, Hiroshi Nakagawa, Masahiro Aoyagi, and Kohji Koshiji, " Investigation of Optimized High-Density Flip-Chip Interconnect Design including Micro Au Bumps for 3-D Stacked LSI Packaging", National Institute of Advanced Industrial Science and Technology (AIST), Ibaraki, Japan, and Tokyo University of Science, Chiba, Japan
- M. Aoyagi, N. Watanabe, M. Suzuki, K. Kikuchi, S. Nemoto, N. Arima, M. Ishizuka, Y. Suzuki, T. Shiomi," New Optical Three Dimensional Structure Measurement Method of Cone Shape Micro Bumps Used for 3D LSI Chip Stacking", National Institute of Advanced Industrial Science and Technology (AIST), Ibaraki, Japan, and SoftWorks Co. Shizuoka, Japan
- Bei Zhang, Baohu Li, and Vishwani D. Agrawal, "Yield Analysis of a Novel Wafer Manipulation Method in 3D Stacking", Department of Electrical and Computer Engineering Auburn University, Auburn, AL,
- Gérald Cibrario, David Henry, Chantal Chantre, Robert Cuchet, Audrey Berthelot, Karim Azizi-Mourier, Marjorie Gary, and Fabien Gays, "A 3D Process Design Kit Generator Based On Customizable 3D Layout Design Environment", CEA- Leti, Grenoble, France
- K. Ghosh, C.C. Yap, B. K. Tay, and C. S. Tan, "Integration of CNT in TSV (≤ 5 μm) for 3D IC Application and Its Process Challenges", School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore
- Mohammad A. Ahmed, M. Chrzanowska-Jeske, "TSV Capacitance Aware 3D Floorplanning", Electrical and Computer Engineering, Portland State University, Portland OR
- Nahid Hossain, Munim Hossain, Abdul Hamid Bin Yousuf, and Masud H Chowdhury, "Thermal aware Graphene Based Through Silicon Via Design for 3D IC", Computer Science and Electrical Engineering, University of Missouri, Kansas City, MO
- Daniel H. Jung, Jonghyun Cho, Heegon Kim, Jonghoon J. Kim, Hongseok Kim, Kwang-Seong Choi, Hyun-Cheol Bae, and Joungho Kim, "Fault Isolation of Short Defect in Through Silicon Via (TSV) based 3D-IC", Terahertz Interconnection and Package Laboratory, KAIST, South Korea, and IT Materials and Components Laboratory, ETRI, South Korea
- Laura B. Mauer, Stephen P. Olson, Elena Lawrence, Ramey Youssef, and John Taddei, "Silicon Etch with Integrated Metrology for Through Silicon Via (TSV) Reveal", Solid State Equipment Horsham, PA, and SEMATECH, Albany, NY

- Jae Hak Lee, Hyoung Joon Kim, Jun-Yeob Song, Chang Woo Lee, Tae Ho Ha," A Study on Wafer Level TSV Build-Up Integration Method", Korea Institute of Machinery and Materials, Daejeon, Korea
- M. Murugesan, H. Wang, K.W. Lee, Y. Sutou, J.C. Bea, T. Fukushima, T. Tanaka, J. Koike, and M. Koyanagi, "Effect of CVD Mn Oxide Layer as Cu Diffusion Barrier for TSV", New Industry Creation Hatchery Center, Tohoku University, Japan, Department of Material Science and Engineering, Tohoku University, Japan, and Department of Biomedical Engineering, Tohoku University, Japan
- Manjari Pradhan, Chandan Giri, Hafizur Rahaman, and Debesh K. Das, "Optimal Stacking of SOCs in a 3D-SIC for Post-Bond Testing", Dept. of Computer Science, Jadavpur University, Jadavpur, India, and Bengal Engineering and Science University Shibpur, Howrah, India
- T. Fukushima, J. Bea, M. Murugesan, K.-W. Lee, and M. Koyanagi, "Development of Via-Last 3D Integration Technologies Using a New Temporary Adhesive System", New Industry Creation Hatchery Center, Tohoku Univ., Japan, and Global Integration Initiative (GINTI), Tohoku Univ., Japan
- A. Ikeda, L.J. Qiu, K. Nakahara, and T. Asano, "Surface Passivation of Cu Cone bump by Self-Assembled-Monolayer for Room Temperature Cu-Cu Bonding", Kyushu University, Fukuoka, Japan
- J. Zhang, L. Zhang, Y. Dong, H.Y. Li, C. M. Tan, G. Xia, and C. S. Tan, "The dependency of TSV keep-out zone (KOZ) on Si crystal direction and liner material", Nanyang Technological University; Singapore, Institute of Microelectronics, A*STAR, Singapore, and University of British Columbia, Canada
- Thomas Uhrmann, Thorsten Matthias, Juergen Burggraf, Daniel Burgstaller, Markus Wimplinger, Harald Wiesbauer, and Paul Lindner, "Recent Progress in Thin Wafer Processing", EV Group, Florian Inn, Austria
- Jubee Tada, Ryusuke Egawa, and Hiroaki Kobayashi, "Design of a 3-D Stacked Floating-Point Adder", Graduate School of Science and Engineering, Yamagata University, Yonezawa, Japan, Research Division on Supercomputing Systems, Cyberscience Center, Tohoku University, and JST CREST
- Jui-Chin Chen, John H. Lau, Tzu-Chien Hsu, Chien-Chou Chen, Pei-Jer Tzeng, Po-Chih Chang, Chun-Hsien Chien, Yiu-Hsiang Chang, Shang-Chun Chen, Yu-Chen Hsin, Sue-Chen Liao, Cha-Hsin Lin, Tzu-Kun Ku, and Ming-Jer Kao "Challenges of Cu CMP of TSVs and RDLs Fabricated from the Backside of a Thin Wafer", Industrial Technology Research Institute, Hsinchu, Taiwan
- Dipanjan Gope, Sourav Chatterjee, Daniel de Araujo, Swagato Chakraborty, James Pingenot, and Raúl Camposano, "Device Physics aware 3D Electromagnetic Simulation of Through-Silicon-Vias in System Modeling", Indian Institute of Science, Bangalore, India, and Nimbic Inc., Mountain View, CA
- R. Fuentes, "Wafer Thinning for 3D Integration", Materials and Technologies, Corp, Wappingers Falls, NY
- Nyunyi M. Tshibangu, Paul D. Franzon, Eric Rotenberg, and William R. Davis, "Design of Controller for L2 Cache Mapped in Tezzaron Stacked DRAM", Department of Electrical and Computer Engineering, NC State Univ. Raleigh, NC
- Awet Yemane Weldezion, Matt Grange, Dinesh Pamunuwa, Axel Jantsch, and Hannu Tenhunen, "A Scalable Multi-Dimensional NoC Simulation Model for Diverse Spatio-temporal Traffic Patterns", KTH Royal Institute of Technology, Kista, Sweden; Mentor Graphics, Wilsonville, Oregon and University of Bristol, Bristol, UK

- L. Yavits, A. Morad, and R. Ginosar," 3D Cache Hierarchy Optimization", Department of Electrical Engineering, Technion – Israel Institute of Technology, Haifa, Israel
- K. Kiyoyama, Y. Sato, H. Hashimoto, K-W Lee, T. Fukushima, H. Kobayashi, T. Tanaka, and M. Koyanagi, "A Block-Parallel ADC with Digital Noise Cancelling for 3-D Stacked CMOS Image Sensor", Dept. of Electrical and Electronics Engineering, Nagasaki Institute of Applied Science, 536 Aba-machi, Nagasaki, Japan, New Industry Creation Hatchery Center, Tohoku University, Japan , Graduate School of Biomedical Engineering, Tohoku University, Japan, and Association of Super-Advanced Electronics Technologies (ASET), Japan
- Jun-Yeob Song, Jae Hak Lee, Hyoung Joon Kim, Chang Woo Lee, and Tae Ho Ha," High Reliability Insert-Bump Bonding Process for 3D Integration", Korea Institute of Machinery and Materials, Korea
- Sayuri Kohara, Akihiro Horibe, Kuniaki Sueoka, Keiji Matsumoto, Fumiaki Yamada, Hiroyuki Mori, and Yasumitsu Orii, "Thermo-mechanical evaluation of 3D packages", IBM Research-Japan, Kanagawa, Japan
- Jiacheng Wang, Shunli Ma, Sai Manoj P. D., Mingbin Yu, Roshan Weerasekera, and Hao Yu, "High Speed and Low Power 2.5D I/O Circuits for Memory-logic-integration by Through-Silicon Interposer", Nanyang Technological University, Singapore; Fudan University, China, and Institute of Microelectronics, A*STAR, Singapore
- Andy Heinig, "Layout dependent Synthesis for Manufacturing Costs optimized 3D Integrated Systems", Fraunhofer Institute for Integrated Systems, Dresden, Germany
- Edward J. Suh, and Paul D Franzon, "Design of 60 GHz Contactless Probe System for RDL in Passive Silicon Interposer", Electrical and Computer Engineering, NC State University, Raleigh, NC
- Frank Windrich, and Andreas Schenke, "Front to backside alignment for TSV based 3D integration", Fraunhofer IZM "All Silicon System Integration Dresden"-ASSID, Moritzburg, Germany
- Chun-Hsien Chien, Hsun Yu, Ching-Kuan Lee, Yu-Min Lin, Ren-Shin Cheng, Chau-Jie Zhan, Peng-Shu Chen,Chang-Chih Liu, Chao-Kai Hsu, Hsiang-Hung Chang, Huan-Chun Fu, Yuan-Chang Lee, Wen-Wei Shen, Cheng-Ta Ko, Wei-Chung Lo, and Lu,Yung Jean, "Performance and Process Characteristic of the Glass interposer with Through-Glass-Via (TGV)", Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, and Corning , Corning, NY
- Tomasz Bieniek, Grzegorz Janczyk, Rafał Dobrowolski, Dariusz Szmigiel, Magdalena Ekwińska, Piotr Grabiec, Janus Paweł, and Jerzy Zając1, "Dedicated MEMS-based test structure for 3D SiP interconnects reliability investigation", Division of Silicon Microsystem and Nanostructure Technology, Instytut Technologii Elektronowej (ITE), Warsaw, Poland, Instytut Technologii Elektronowej (ITE), Warsaw, Poland, and Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Warszawa, Poland
- Yang Yi, and Yaping Zhou, "A Novel Circuit Model for Multiple Through Silicon Vias (TSVs) in 3D IC" University of Missouri , Kansas City, MO; NVidia Corporation, Santa Clara, CA
- Jonghoon J. Kim, Heegon Kim, Daniel H. Jung, Sunkyu Kong, Sukjin Kim, Bumhee Bae, Junho Lee, Kunwoo Park, and Joungho Kim, "Non-Contact Wafer-Level TSV Connectivity Test Methodology Using Magnetic Coupling", Terahertz Interconnection and Package Laboratory, KAIST, Korea, and Advanced Design Team, SK Hynix Semiconductor Inc., Korea
- Surajit Kumar Roy, Sobitri Chatterjee, Chandan Giri, and Hafizur Rahaman, "Faulty TSVs Identification and Recovery in 3D Stacked ICs During Pre-bond Testing", Bengal Engineering and Science University, Howrah, India

- S.Nishizawa, R.Arima, F.Inoue, T.Shimizu, and S.Shingubara, “Highly Conformal and Adhesive Electroless Barrier and Cu Seed Formation using Nanoparticle Catalyst for Realizing a High Aspect Ratio Cu-filled TSV”, Graduate School of Engineering, Kansai University, Osaka, Japan, and Tohoku University, Japan
- Onnik Yaglioglu , and Ben Eldridge, “Contact Testing of Copper Micro-pillars with Very Low Damage for 3D IC Assembly”, FormFactor Inc., Livermore, CA, USA
- Gopi Neela, and Jeffrey Draper, “Techniques for Assigning Inter-Tier Signals to Bondpoints in a Face-to-Face Bonded 3DIC”, Information Sciences Institute, University of Southern California, Los Angeles, CA
- Caleb Serafy, Bing Shi, Ankur Srivastava, and Donald Yeung, “High Performance 3D Stacked DRAM Processor Architectures with Micro-Fluidic Cooling”, Department of Electrical and Computer Engineering, University of Maryland, College Park, Maryland
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